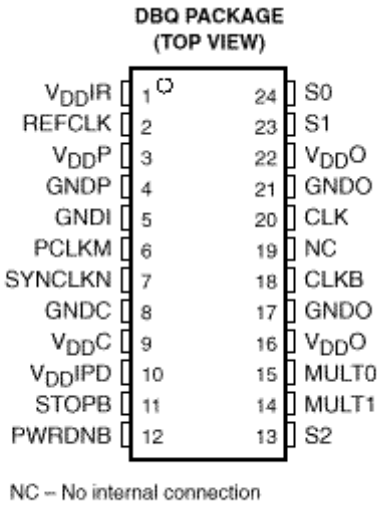
Advanced Information

CDCR81
DIRECT RAMBUS(TM) CLOCK GENERATOR
FOR PC MOTHERBOARDS
SEPTEMBER 1998

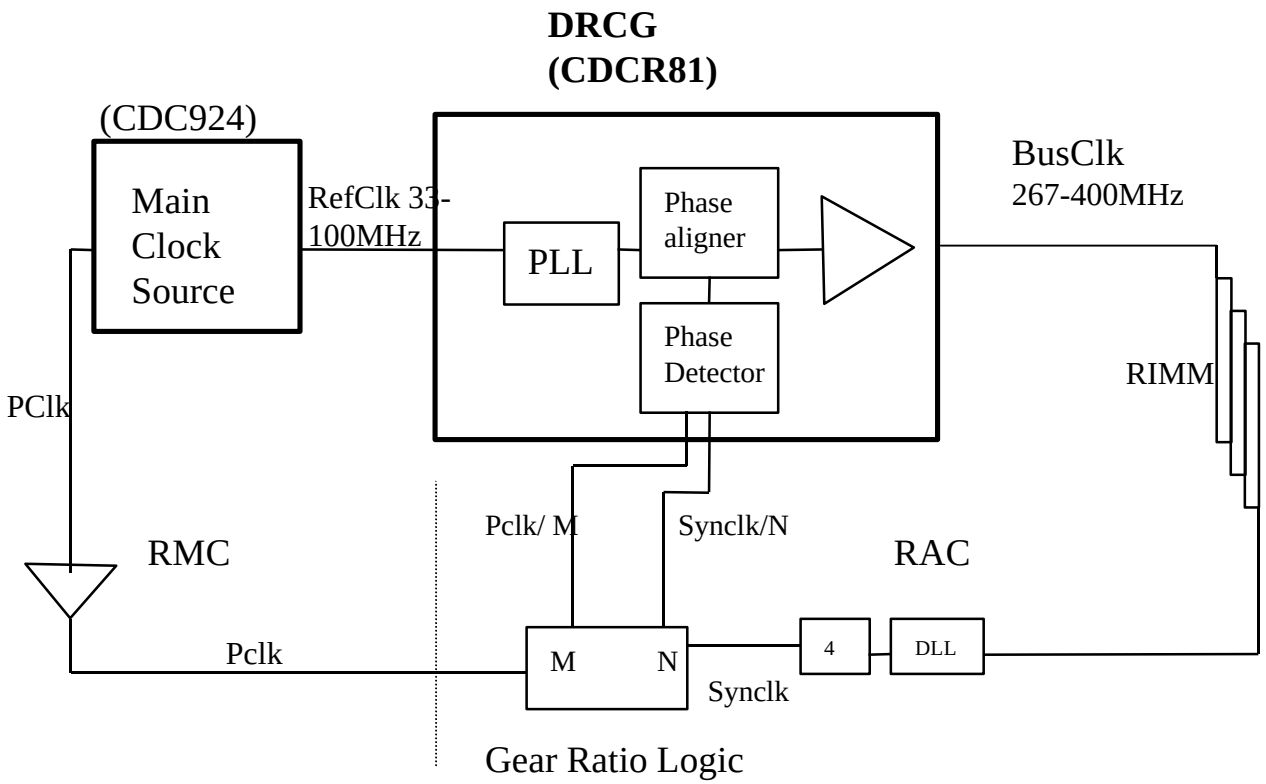
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **400-MHz Differential Clock Source for Direct Rambus (TM) Memory Systems for an 800-MHz Data Transfer Rate**
- **Synchronizes the Clock Domains of the Rambus (TM) Channel With an External System or Processor Clock**
- **Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications**
- **Operates from a Single 3.3-V Supply**
- **Packaged in a Shrink Small-Outline Package (DBQ)**
- **Wide Phase-Lock Input Frequency Range 33 MHz to 67 MHz**
- **No External Components Required for PLL**
- **Supports Independent Channel Clocking**
- **Spread Spectrum Clocking Tracking**
- **Capability to Reduce EMI description**

The Direct Rambus clock generator (DRCG) provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLK/M = SYNCLK/N, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLK/M and SYNCLK/N and adjusts the phase of BUSCLK such that the skew between PCLK/M and SYNCLK/N is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency. User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 400 MHz with clock references ranging from 33 MHz to 67 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass, the PLL and REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.



DRCG system architecture



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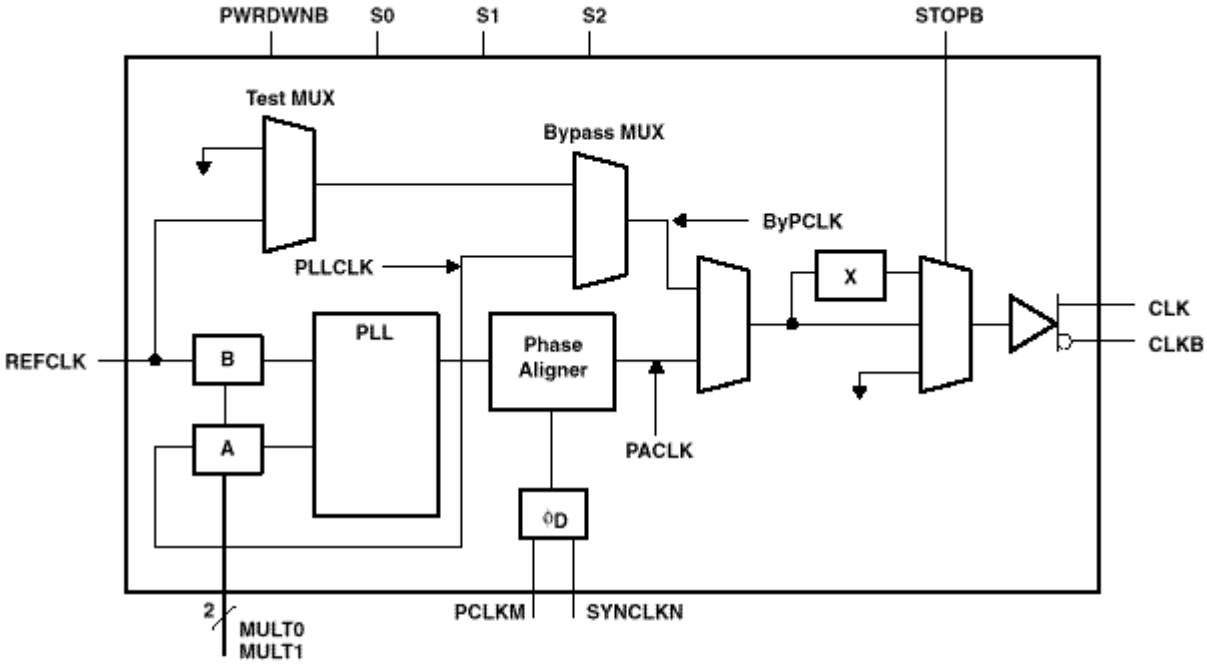
functional block diagram



FUNCTION TABLE†

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output Test (OE)	0	1	X	Z	Z
Reserved	0	0	1	Divided by N	Divided by N
Reserved	1	0	1	PD BIST	PD BIST
Reserved	1	1	1	–	–

† X = don't care, Z = high impedance

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
$V_{DD}C$	9		V_{DD} for phase aligner
$V_{DD}IPD$	10		Reference voltage for phase detector inputs and STOPB
$V_{DD}IR$	1		Reference voltage for REFCLK
$V_{DD}O$	16, 22		V_{DD} for clock outputs
$V_{DD}P$	3		V_{DD} for PLL

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PLL divider selection

The Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that 267 MHz <BUSCLK <400 MHz and REFCLK < 100 MHz.

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)	INTERNAL DIVIDER N
0	0	67	4	267	8
0	1	50	6	300	24
0	1	67	6	400	16
1	1	33	8	267	16
1	1	50	8	400	16
1	0	100	8/3	267	16

clock output driver states

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK Stop	1	0	$V_{X, STOP}$	$V_{X, STOP}$
Normal	1	1	PACLK/PLLCLK/ REFCLK†	PACLK/PLLCLK/ REFCLK

† Depending on the state of S0, S1, and S2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to 4 V
Output voltage range, V_O, at any output terminal . . . . . –0.5 V to V_{DD} + 0.5 V
Input voltage range, V_I, at any input terminal . . . . . –0.5 V to V_{DD} + 0.5 V
ESD rating . . . . . TBD
Continuous total power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.