

2 Architectural Overview

This section describes the basic functions of a MSP430 based system.

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The MSP430 devices contain the following main functions:

- Central Processing Unit (CPU)
- Program Memory (ROM or EPROM)
- Data Memory (RAM or EEPROM)
- Control of operation
- Peripheral Modules
- Oscillator + Frequency Multiplier.

The architecture of the MSP430 family is based on a memory-to-memory architecture, a common address space for all functional blocks, and a reduced instruction set applicable for all functional blocks.

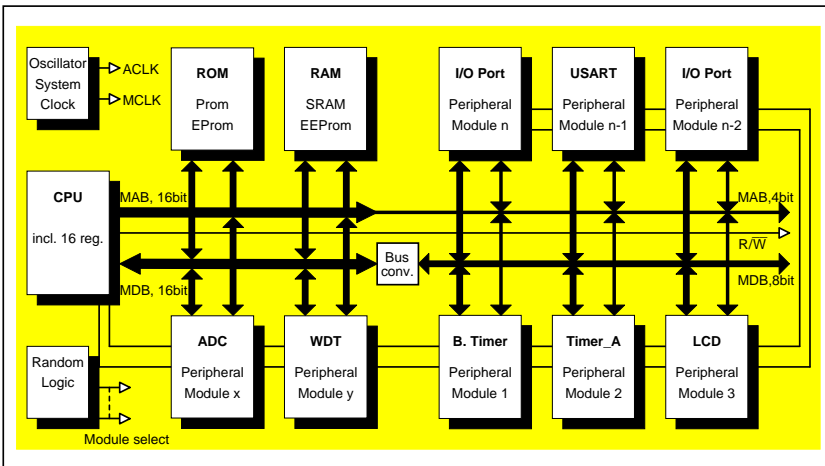


Figure 2.1: MSP430 system configuration

2.1 CPU

The central processing unit incorporates the following reduced, highly transparent instruction set, and a highly orthogonal design. It consists of a sixteen bit ALU, sixteen registers and an instruction control logic. Four of these registers are used for special purposes, these are the Program Counter PC, Stack Pointer SP, Status Register SR and Constant Generator CG2. All registers - except R3/CG2 and part of R2/CG1- can be used as general-purpose registers applying the complete instruction set to registers. The constant generator supplies constants for performing the instruction not for storing any data. The addressing mode used on CG1 separates the data of the constants.

The complete control over the Program Counter, the processor's Status Register and the Stack Pointer with the reduced instruction set, allows the development of applications with complex addressing modes or SW algorithms.

2.2 Code Memory

Access to the Code Memory is always word organized for fetching code, data can be read with word or byte access. Any access uses the 16-bit Memory Data Bus and as many of the least significant address lines as are needed to access the memory locations. Blocks of memory are automatically selected via Module Enable signals, this being a technique to reduce overall current consumption. Program memory can be integrated as programmable (EPROM) or mask programmable (ROM) memory. Standard members of the MSP430 family support OTP and mask programmed versions. Support of external memory will be the subject of future enhancements.

Sixteen words of memory are reserved for reset and interrupt vectors at the top of the lowest 64K byte address space from 0FFFFh down to 0FFE0h.

Access to Program Memory via software program is fully supported for read operation (MOV &0FFA0h,R5), but not for write (→ ROM).

Future enhancements:

The address space will be enhanced using segmented memory areas. The expanded addressable space is supported mainly using three extensions: branch and call long instructions, code segment pointer CSP and data pointer DPP. The code segment pointer is located within the status register SR. This enhanced address space is used for instruction codes (CSP + PC) and for data memory ([DPPi] + operand address) as follows:

MAB = CSP * 1000h + PC during any access to code memory

MAB = DPPi * 400h + Rs/d during any access to stack or data memory

For basic devices using up to 64K byte addressing space, the content of CSP and DPP is unused by the Memory Address Bus.

2.3 Data Memory (RAM)

The Data Memory is connected to the CPU via two busses: the Memory Address Bus (MAB), and the Memory Data Bus (MDB). The Data Memory can be integrated into the specific family member either with full (word) data width or with reduced (byte) data width.

The entire instruction set operates fully on byte and word data. All operations on stack and PC are word operations, and should use only even aligned addresses.

2.4 Control of operation

The operations of the different MSP430 members are controlled mainly with the information stored in special function registers, SFRs. The different bits in the SFRs enable interrupts, support the software on the status of the interrupt flags and define the operating modes of the peripherals. Peripherals that are disabled stop their functional operation to reduce current consumption. All data stored in the module's register are retained. Peripherals that have their operating mode controlled can be identified in the specific sections.

2.5 Peripherals

Peripheral modules are connected to the CPU via Memory Address Bus MAB, Memory Data Bus MDB and interrupt service and request lines. The MAB is usually a 5-bit bus for most of the peripherals. The MDB is an 8-bit or 16-bit bus. Modules with an 8-bit data bus are connected via bus conversion circuitry to the 16-bit CPU. The data exchange with these modules should be handled with byte instructions, without exception. Instruction execution on word-oriented peripherals operates without any restrictions. Most of the peripherals are operating in byte format. The SFRs are handled within an 8-bit data range without any exception. The operation to 8-bit peripherals follows the orders described.

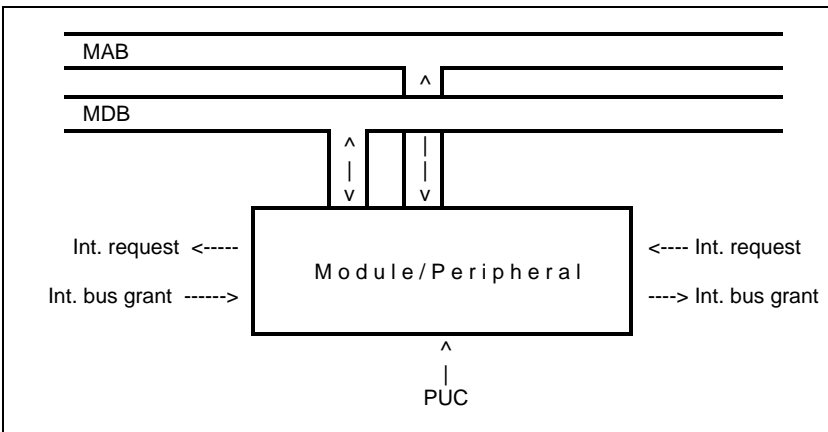


Figure 2.2: Bus connection of modules/peripherals

2.6 Oscillator, Frequency Multiplier and Clock Generator

The oscillator is specially designed for the commonly-used clock crystal of 32,768 Hz with low current consumption. All analog components are integrated; only the crystal has to be connected.

This oscillator is the direct source for some modules with low-frequency requirements. For the CPU and other modules, the crystal's frequency is multiplied by a first order frequency lock loop circuitry FLL. The FLL starts after power-up with its lowest possible frequency, and is regulated to the proper frequency by controlling a digital controlled oscillator DCO.

The long-term deviation is limited by the stability of the crystal and oscillator.

The frequency of the clock generator for the processor's operation is a fixed multiple of the crystal, and supports the clock MCLK.