7 Oscillator and System Clock Generator

The oscillator and the system clock generator follow the major targets of low system cost and low power consumption.

External component count is reduced down to a commonly used crystal to achieve the target of low system cost. The use of a low frequency crystal and oscillator combined with a multiplier meets system cycle speed and the second target of low power consumption.

Features for current limited applications

Special other features are obviously mandatory in very low power consuming devices that use the various extended operating modes. These features include startup timing, long term frequency stability with voltage, temperature and time, and a highly-stable time base for real time clocks.

Current limited real-time applications demand two conflicting requirements: low system clock frequency for energy conservation, and high system clock frequency for fast reaction to requesting events. Especially battery based applications are very critical with respect to current consumption. Response to external events or time requests typically requires occasionally high speed in real-time applications.

A processor clock generator with fast start-up allowing exhaustive use of different power dissipation modes could theoretically solve this dilemma. On the other hand, fast start-up is closely combined with unacceptably low frequency stability. Design with multiple clock sources or different clock operations could take into account the clock requirements of certain peripheral components for real-time applications such as low frequency communication, display (e.g. LCD), timers and counters.

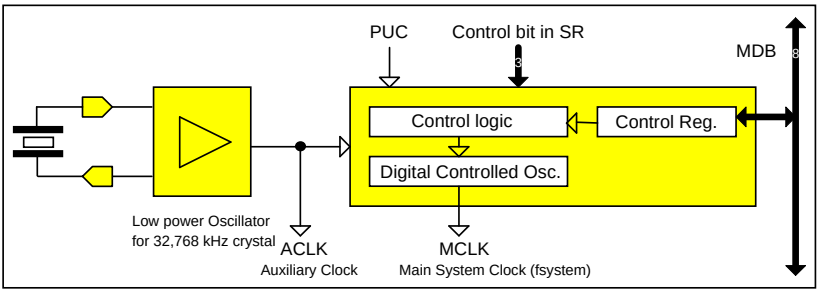


Figure 7.1: Principle of Clock Generation

The output of the low frequency crystal oscillator provides the clock signals for the CPU operation and the peripheral modules. The oscillator of the MSP430 operates with the widely used crystal, without any external components.

The different requirements of CPU and modules, from the point of view of current consumption objectives, requires the use of two clock signals:

- Auxiliary Clock ACLK with crystal's frequency
- System Clock MCLK with a higher frequency: N x $f_{crystal}$.

7.1 Crystal Oscillator

The special design of the oscillator supports the features of low current consumption and the use of a 32 768Hz crystal. The crystal is connected to two pins without any other external components. All components for stabilizing the operation state or phase shifter capacitors are integrated.

Two factors dominate the choice of the well-known and widely used watch crystal:

- oscillator and time base for low current consumption
- optimize system costs.

The oscillator starts operating after applying VCC due to reset of the control bit OscOff in the Status Register SR. It can be stopped by setting the OscOff bit.

15	8	7							0
reserved for future enhancements	V	SCG 1	SCG 0	Osc Off	CPU Off	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Figure 7.2: Status Register SR

7.2 Processor Clock Generator

The System Clock of controllers has to meet different requirements, according to the application and system conditions:

- High frequency, to react fast onto system hardware requests or events
- Low frequency, to minimize current consumption, EMI, ...
- Stable frequency for timer applications e.g. real time clock RTC
- Low-Q oscillators to enable start-stop operation with 'zero' delay to operation.

All the conflicting but essential requests can not be handled, either with high-Q, fast frequency crystals, or with low-Q RC-type oscillators. Proper current consumption and the frequency stability mentioned require the use of a low frequency crystal. The compromise used in the MSP430 is to use a low frequency crystal, and to multiply its frequency up to the nominal operating range:

$$f_{System} = N \times f_{crystal}$$

Different ways for multiplication of the crystal's frequency to the system frequency are known, and several are practiced. The most known methods are the Phase-Locked-Loop PLL technique, and Frequency-Locked-Loop FLL.

The PLL technique has two major disadvantages in systems with frequently and time-undefined intermitted operating modes. PLL's are systems following second order response. All the on-off operating modes result in out-of-phase conditions, and therefore in continuous 'limp-mode' handling. The wide ranges of off-time conditions conflict with the use of analog filter-integrators in the closed loop. Changes in the capacitor's charge automatically result in phase and/or frequency deviations and an improper frequency until the system is in phase.

The FLL technique, in combination with a digital controlled oscillator (DCO), avoids both serious problems.

The major features of the DCO are:
- fast start-up
- digital (not analogs) control signals.

Beside these advantages one item needs careful consideration: the variation of the frequency with the supply voltage and temperature.

The DCO is absolutely monotone.

The FLL operates as a continuous frequency integrator. An up/down counter that follows the loop control corrects permanently the multiplication factor N. The follow-up or up-date rate is identically to the crystal's frequency rate. Using a 32,768 kHz crystal the rate is 30.5µs.

The accumulated frequency error is the same as that of the crystal's. The time deviation from one machine cycle to another is typically less than 10%.

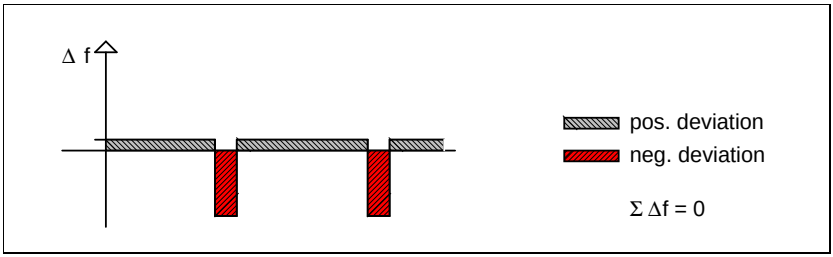


Figure 7.3: System frequency vs. time

The start-up operation of the system clock depends on the previous machine state. During a PUC the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after removing the PUC condition. Proper working condition for the control logic needs the presence of stable crystal oscillation.

The frequency integrator of 10bit length controls the frequency at which the DCO is running with. The integrator - starting at zero digital value after PUC - counts up to run the frequency f_{System} at the selected value N. It takes slightly more periods of the crystal input than the suggested number of 10bit or 1024, if the maximum length of the frequency integrator is needed. The control logic system operates aperiodically.

Applications that run the controller with intermitted operation need some attention to the conditions of handling the system frequency control conditions. The correction of the frequency integrator is possible each period of the crystal (30.5 µs @ 32,768 Hz) plus the period of f_{System}/N. Longer integration periods are mandatory to avoid accumulating deviations in time.

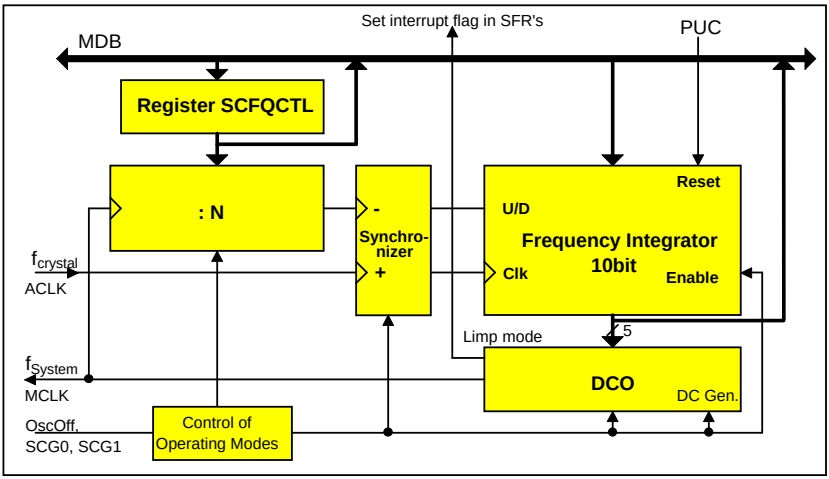


Figure 7.4: Schematic of system frequency generator

Two flags are incorporated in the special function register which allow the application program to get back control over the system, if the digital controlled oscillator is at its upper or lower frequency limit.

The operation at the upper or lower limit can be easily detected by controlling the frequency integrator via access to SCFI0 and/or SCFI1.

7.3 System Clock Operating Modes

The system clock generator and crystal oscillator are controlled by three signals. These signals are located in the status register SR and are reset during the four different power-up conditions.

These three control signals provide the system application with different operating conditions and maximum flexibility to optimize overall system power consumption. During some combinations of the three control signals the system clock MCLK stops operation; the existing value of the frequency integrator remains.

SCG1	SCG0	OscOff	Crystal oscillator	DC Generator	DCO	Loop control	Comments
0	0	0	ON	ON	ON	ON	Condition after PUC Crystal and DC oscillator are active Loop control is operating
0	1	0	ON	ON	ON	OFF	Low Power Mode **LPM1** Crystal and DC oscillator are active Loop control is off
1	0	0	ON	ON	OFF	OFF	Low Power Mode **LPM2** Crystal oscillator and DC Generator are active DCO and Loop control are off
1	1	0	ON	OFF	OFF	OFF	Low Power Mode **LPM3** Crystal oscillator is active All other functions are off
X	X	1	OFF	OFF	OFF	OFF	Low Power Mode **LPM4** All functions are disabled $f_{MCLK} = f_{ACIk} = 0Hz$

The three control signals provide five different power down modes, supporting ultra-low power applications, by making intensive use of them. All these different modes provide the system application with the potential for operation with the smallest time slot possible, and the optimized current consumption in each time slot.

The SCG0 bit controls the FLL loop if it is operating (SCG0 is reset) or off (SCG0 is set).

Starting from PUC
The system clock control register SCFQCTL is set to 01Fh with PUC, and the frequency integrator is reset. The reset of the frequency integrator sets the system frequency to its lowest value, and counts up continuously until it locks at a system frequency that is equal to N times the crystal frequency.

Low Power Mode LPM4, Oscillator off
During the oscillator off mode all parts of the processor are inactive, and the current consumption is at its lowest limit. Starting with operation is only possible after power-up circuitry has detected a low supply voltage condition or any external interrupt event that will request an interrupt asynchronously. The appropriate enable for interrupt sources should be applied during the program flow.

The start-up sequence of the system clock generator out of oscillator off mode:
- the present system frequency defined by the output value of the frequency integrator and the DCO characteristic will continue running
- the frequency integrator is continuously counted down with the frequency of f_{System}/N till the DCO is running at its lowest frequency as long as the crystal oscillator has not started operation
- after the crystal oscillator starts operation, the loop control will settle the frequency integrator to the value following $f_{System} = N * f_{crystal}$.

Low Power Mode LPM3, DC Generator off
During the DC generator off mode only the crystal oscillator is active. The DC current of the DC generator that sets the basic timing conditions is switched off. The power consumption constraints force high impedance design. The start of the DCO from power-down mode with DC generator off can take some time (t_{DCGon}) to run with the selected frequency. The time is in the range between ns up to µs.

Low Power Mode LPM2, DCO off
The crystal oscillator and the DC generator are still active during LPM2, and an immediate start is possible. The start-up delay is limited to some gate delays.

Low Power Mode LPM1, Frequency-lock-loop off
The crystal oscillator, the DC generator and the DCO are still active during LPM1. The processor with all its peripheral modules is fully functional without any limitation. The frequency is determined from the output value of the frequency integrator. This value, with the characteristic of the DCO, determines the frequency of the MCLK signal that is identical to the system frequency f_{System}.
There is no start-up delay: the oscillator is already running. The loop control is activated asynchronously and with a slight frequency variation, but it settles fast and aperiodically.

7.4 System Clock Control Register

The system clock generator interacts with other processor parts via three general module registers and the special function registers. The general module registers are mapped into the lower peripheral file address range where all byte modules are located. Three control lines for the operating states, SCG1, SCG0 and OscOff, are supplied from the status register SR of the CPU.

7.4.1 General Module Registers

Two eight bit registers control the system clock generator. The user's software loads one of the registers with the multiplication factor N. The other register holds control bits or signals used for various operating modes. It should be accessed using byte instructions.

System Clock Frequency Control

SCFQCTL
052h

7							0
M	2^6	2^5	2^4	2^3	2^2	2^1	2^0
rw-0	rw-0	rw-0	rw-1	rw-1	rw-1	rw-1	rw-1

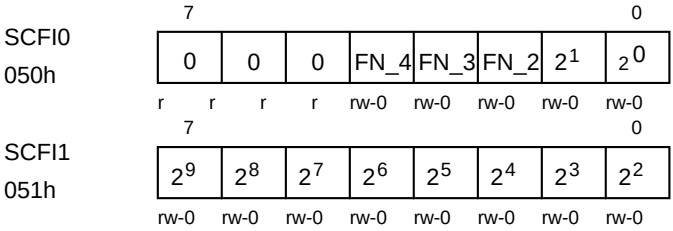
The content of register SCFQCTL controls the multiplication of the crystal's frequency. The seven bits indicates a range of 3+1 to 127+1.

$$f_{System} = (x*2^6 + x*2^5 + x*2^4 + x*2^3 + x*2^2 + x*2^1 + x*2^0 + 1) * f_{crystal}$$

The default value in SCFQCTL after PUC was active is 31, which results in a factor of 32.
The range of the f_{System} is theoretical and depends on the adjustable frequency range of the DCO (see more information in electrical characteristics).

> **Note: Multiplication factor in SCG**
>
> The content of register SCFQCTL (2^6 to 2^0) controls the multiplication of the crystal's frequency. The seven bits must be in the range of 3 to 127. Any value below 3 results in unpredictable operation, but also any value than 127 will force the MCLK frequency above the device specification.

System Clock Frequency Integrator



The output of the frequency integrator controls the DCO. This value can be read using the appropriate address of SCFI1 and SCFI0. The digital representation is:

$$N_{DCO} = (x* 2^9 + x*2^8 + x*2^7 + x*2^6 + x*2^5) + (1-M)*(x*2^4 + x*2^3 + x*2^2 + x*2^1 + x*2^0)$$

7

SCFI0, Bit 1...3: The three bits in the SC control register 0 define the nominal frequency of the DCO.

FN_4	FN_3	FN_2	Frequency
0	0	0	f_{NOM}
0	0	1	$2 \times f_{NOM}$
0	1	X	$3 \times f_{NOM}$
1	X	X	$4 \times f_{NOM}$

7.4.2 Special function register bits, System Clock Generator related

Two bits in the SFR address range handle the system control interaction according to the function implemented in the SCG. These three bits are:

- OscFault Interrupt Flag OFIFG (located in IFG1.1, initial state is unchanged)
- OscFault Interrupt Enable OFIE (located in IE1.1, initial state is reset).

The interrupt flag is part of a multiple source interrupt request. The same interrupt vector is also used for the event at the $\overline{\text{RST}}$/NMI-pin when NMI function is selected. The interrupt is defined to be non-maskable. Non-maskable implies that the general interrupt enable bit GIE can not disable the interrupt request. Since the interrupt shares the same interrupt vector and an oscillator fault is active after PUC, the interrupt flag is not automatically reset.

Three different situations should be handled by the software:

- After PUC, a proper sequence should be programmed to identify or to set an oscillator condition that prevents active level at OscFault signal, and therefore a permanently set of OFIFG. The OFIFG should be reset by software.
  PUC resets the OFIE bit and no interrupt is requested.

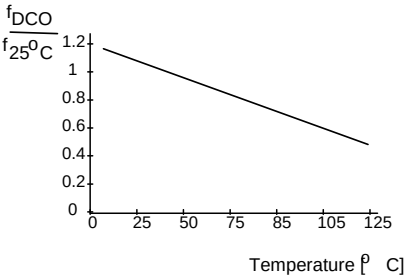
- When an interrupt from the OscFault signal was requested and serviced, the interrupt enable bit OFIE is reset automatically to disable further continuous interrupt requests until proper response from the software conducts to a inactive OscFault signal. After reaching the inactive state, the OFIE bit can be set again following the general rules of module interrupts. An oscillator fault event is not affected by the general interrupt enable bit GIE.
- The interrupt flag OFIFG can be used to identify the interrupt source at the beginning of the interrupt service routine. The OFIFG is set independently of an additional NMI event and is dominant.

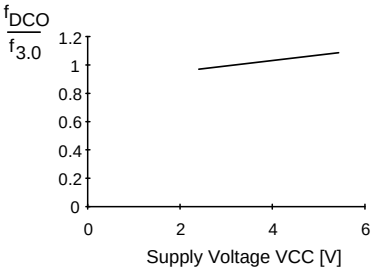
Note: Interrupt flag OFIFG

The interrupt flag OFIFG remains set when an interrupt request has been accepted and serviced. This is mandatory, because it is a multiple source interrupt together with NMI interrupt and it indicates to the software interrupt handle the event of an oscillator fault. Servicing first the OFIFG condition gives this event priority over the NMI event.

7.5 DCO Characteristic - typical

The digital controlled oscillator varies with temperature and supply voltage. Running the frequency loop this is unimportant for the application, because the period of control is identical with the period of the ACLK signal. With a 32,768Hz crystal, it is 30.5µs.





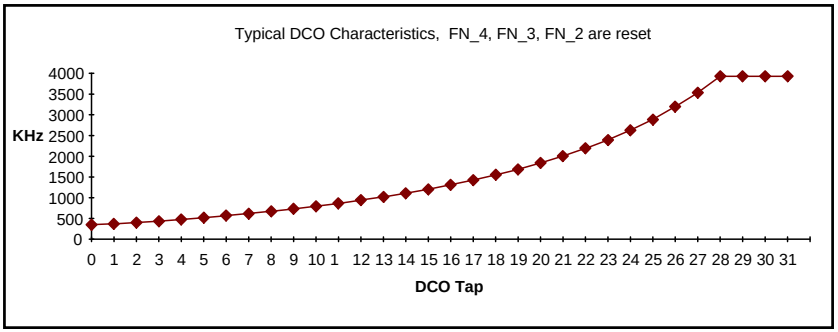


Figure 7.5: DCO Characteristics

Note: DCO Taps

The five most significant bits in the System Clock Frequency Integrator register SCFI1 are feed into the DCO. If the modulation bit M from the register SCFQCTL is set, only the DCO taps are determining the system frequency.