8 Digital I/O Configuration

8.1 General Port P0

The general port P0 incorporates all the functions to individually select the function of each pin and to use each signal as an interrupt source.
The six registers are used for the control of the Port's I/O pins.
The general module registers are mapped into the lower peripheral file address range where all byte modules are located. The register should be accessed with byte instructions, using absolute address mode.

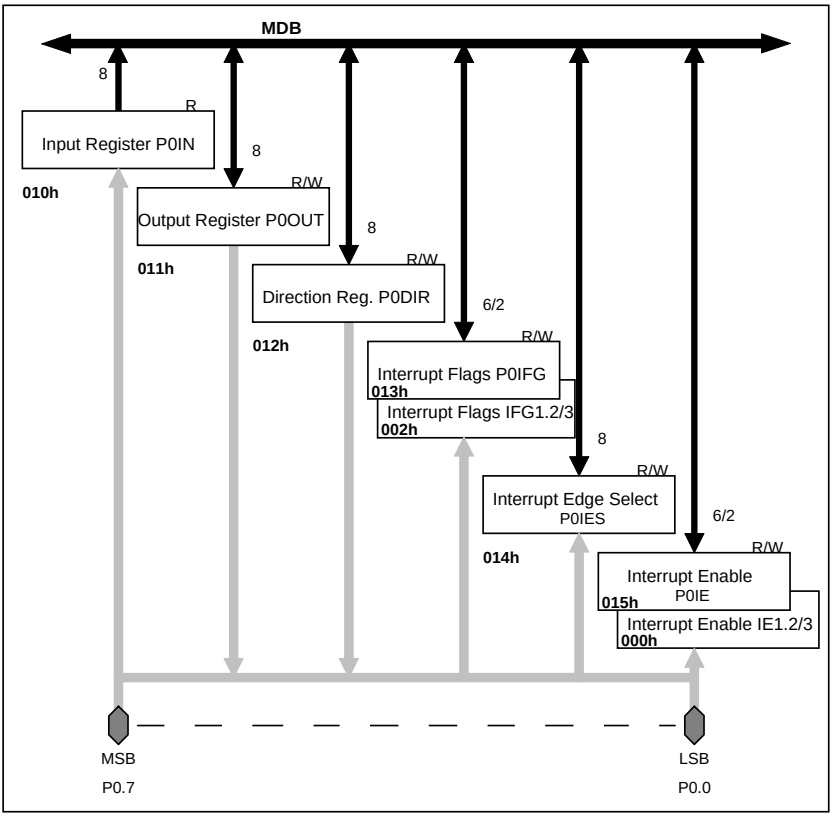


Figure 8.1: Port P0 Configuration

8.1.1 Port P0 Control Registers

The Port P0 is connected to the processor core via the 8-bit MDB structure and MAB. It should be accessed via byte instructions.

The six control registers give maximum flexibility of digital input/output to the application:
- All individual I/O bits are programmable independently:
- Any combination of input, output and interrupt condition is possible.
- Interrupt processing of external events is fully implemented for all eight bits of the port P0.

The six registers are:

Register	short form	Register type	Address	Initial State
• Input register:	P0IN	read only	010h	-----
• Output register:	P0OUT	read/write	011h	unchanged
• Direction register:	P0DIR	read/write	012h	reset
• Interrupt Flags:	P0IFG	read/write	013h	reset
• Interrupt Edge Select:	P0IES	read/write	014h	unchanged
• Interrupt Enable:	P0IE	read/write	015h	reset

All these registers contain eight bits except the two LSBs in the interrupt flag register, and the interrupt enable register. These two bits are included in the special function register SFR. The registers should be accessed with byte instructions.

Input Register P0IN
The input register is a read-only register to scan the signals at the I/O pins. The direction of the pin should be selected for input.

> **Note: Writing to read only register P0IN**
>
> Writing to this read-only register results in an increased current consumption as long as the write is active.

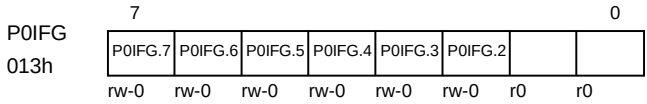
Output Register P0OUT
The Output Register shows the information of the output buffer, an eight bit register that contains the information output at the I/O pins if used as outputs. The output buffer can be modified by all instructions that write to a destination. If read, the contents of the output buffer are read independently of the direction. A direction change does not modify the output buffer contents.

Direction Register P0DIR

This register contains eight independent bits that define the direction of the I/O pin. All bits are reset by PUC:

Bit = 0: The I/O pin is switched to input direction
Bit = 1: The I/O pin is switched to output direction

Interrupt Flags P0IFG
This register contains six flags that contain information if an interrupt is pending or not- according to the corresponding I/O pin:



Bit = 0: No interrupt is pending
Bit = 1: An interrupt is pending due to a transition at the I/O pin. Manipulation on P0OUT and P0DIR can also set bits of P0IFG.

Writing a zero to an Interrupt Flag resets it.
The six flags are located in bit 7 to 2 corresponding to the pins P0.7 to P0.2. The remaining interrupt flags of pin P0.1 and P0.0 are located in the SFRs.

> **Note: Interrupt Flags P0FLG.2...7**
>
> The Interrupt Flags P0FLG.2 to P0FLG.7 use only one interrupt vector: it is a multiple source interrupt vector. The interrupt flags P0IFG.2 to P0IFG.7 are not reset automatically when any interrupt from these events is served. The software decides which event will be served and should reset the appropriate flag.
>
> Any external interrupt event should be as long as 1.5 times MCLK or longer to ensure that it is accepted and the corresponding interrupt flag is set.

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Interrupt Edge Select P0IES
This register contains a bit for each I/O pin that selects which transition triggers the interrupt flag. All eight bits corresponding to pin P0.7 to P0.0 are located in this register. The bits have the following meaning:

Bit = 0: The interrupt flag is set with LO/HI transition
Bit = 1: The interrupt flag is set with HI/LO transition

> **Note: Change of P0IES bit(s)**
>
> Any change of P0IES bit(s) may result in setting the associated interrupt flags.

Interrupt Enable P0IE
This register contains a bit for six I/O pins to enable interrupt request on an interrupt event. Two interrupt enable bits for P0.0 and P0.1 are located in special function register IE1.2 and IE1.3. Six bits corresponding to pin P0.7 to P0.2 are located in the P0IE register.

P0IE
015h

7							0
P0IE.7	P0IE.6	P0IE.5	P0IE.4	P0IE.3	P0IE.2		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r0	r0

The bits have the following meaning:

Bit = 0: The interrupt request is disabled
Bit = 1: The interrupt request is enabled

Note: Port0 interrupt sensitivity

Only transitions, not static levels cause interrupts.

The interrupt routine must reset the multiple-use Interrupt Flags P0IFG.2... P0IFG.7. The single source flags P0IFG.0 and P0IFG.1 are reset when they are serviced.

If an Interrupt Flag is still set (because the transition occurred during the interrupt routine) when the *RETI* instruction is executed, an interrupt occurs again after *RETI* is completed. This ensures, that each transition is seen by the software.

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8.1.2 Port P0 Schematic

Port P0, Bits P0.3 to P0.7
The pin logic of each individual signal of port P0 is built from five identically register bits - P0DIR, P0OUT, P0IFG, P0IE, P0IES - and one read-only input buffer - P0IN. The bits three to seven are identically designed:

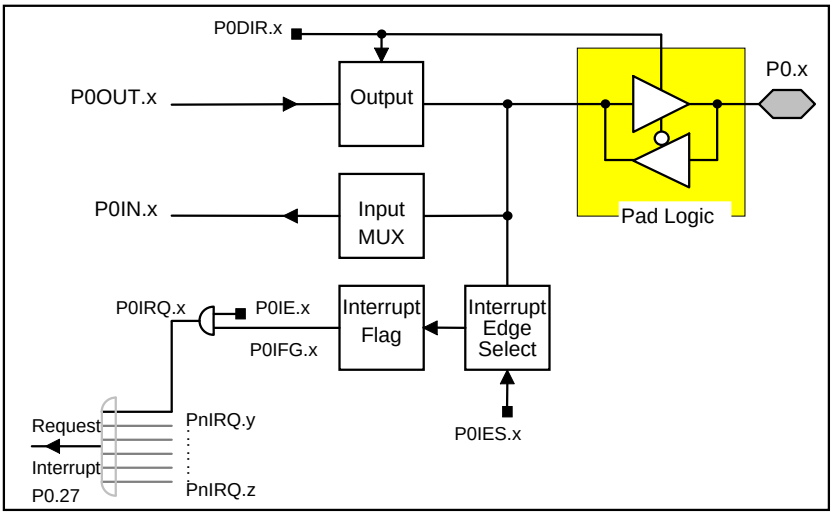

Figure 8.2: Schematic of bits P0.7 to P0.3

The interrupt flag may be set by a relevant input condition, but also by the software. Additionally, when the direction control bit or the interrupt edge select bit are modified a trigger condition may occur.
The port P0 bits two to seven share one common interrupt vector. The interrupt flags are not automatically reset after the P0.27 interrupt request was accepted. The individual flags P0IFG.2 to P0IFG.7 should be reset by software preferably in the corresponding interrupt service routine.

Port P0, Bit P0.2

The bit two is slightly different from bits three to seven. The output signal can be determined either by the port P0OUT.2 bit or by the 8bit Timer/Counter's signal TXD. Whenever output control register bit TXE is set TXD signal is selected to be the relevant output signal and the pad logic is switched to the output, independent of the direction control bit P0DIR.2:

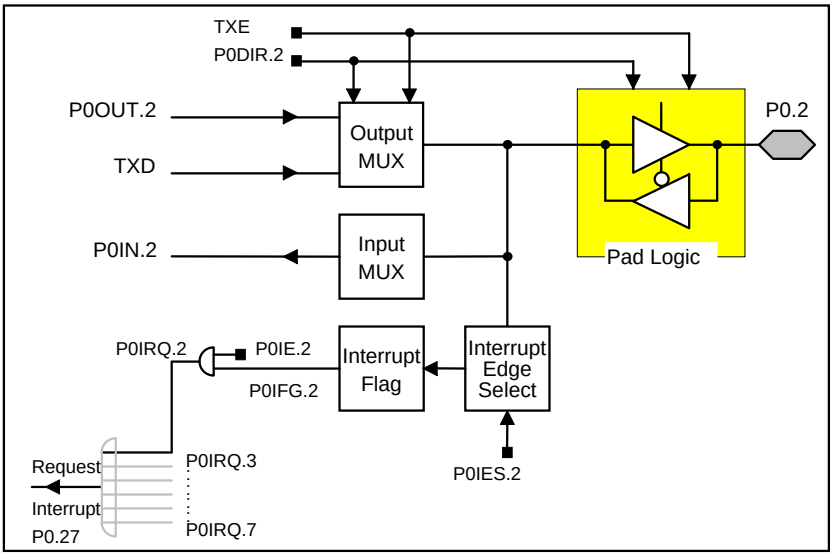

Figure 8.3: Schematic of bit P0.2

The interrupt flag P0IFG.2 shares the interrupt vector with interrupt flags P0IFG.3 to P0IFG.7.

Port P0, Bit P0.1

The bit one is slightly different from bits three to seven. The interrupt signal can be selected to be sourced whether by the input signal at the pin P0.1 or by the 8bit Timer/Counter's signal Carry. Whenever the interrupt source control bit ISCTL in the 8bit Timer/Counter control register TCCTL is set, the interrupt source is switched from the P0.1 pin to the Carry signal from the counter in the 8bit Timer/Counter:

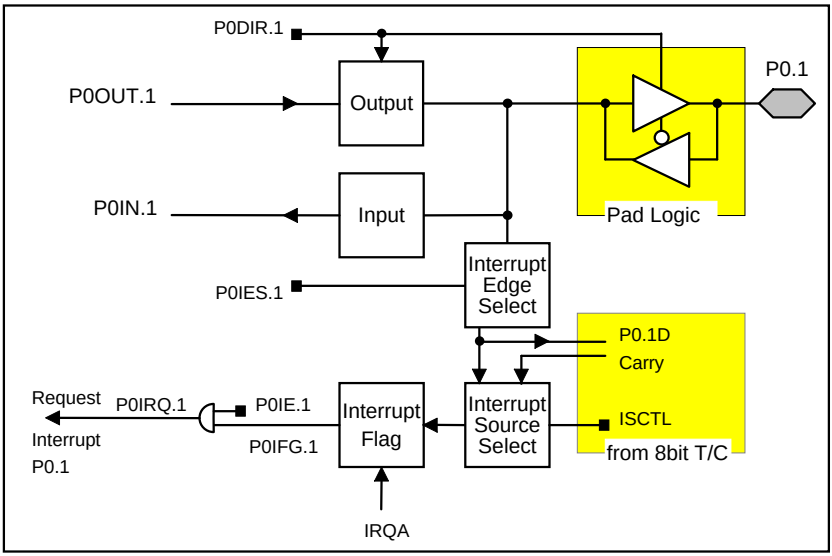

Figure 8.4: Schematic of bit P0.1

The interrupt flag P0IFG.1 is automatically reset when a P0IFG.1 interrupt request was accepted (IRQA).

Port P0, Bit P0.0
The bit zero is identical to bits three to seven, but uses an individual interrupt vector:

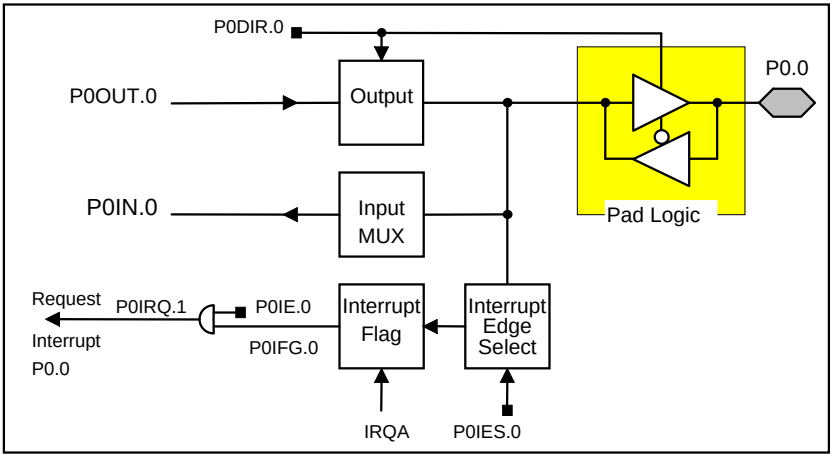

Figure 8.5: Schematic of bit P0.0

The interrupt flag P0IFG.0 is automatically reset when a P0IFG.0 interrupt request was accepted (IRQA).

8.1.3 Port P0 interrupt control functions

Port P0 uses eight bits for interrupt flags, eight bits for interrupt enable, eight bits to select the effective edge of an interrupt event, and three different interrupt vector addresses.
The three interrupt vector addresses are assigned to:
- P0.0
- P0.1/RXD
- P0.2 to P0.7

Two port P0 signals P0.0 and P0.1/RXD are used for dedicated signal processing. Four bits in the SFR address range and two bits in the port0 address frame handle the interrupt events on P0.0 and P0.1/RXD :
- P0.0 Interrupt Flag P0IFG.0 (located in IFG1.2, initial state is reset)
- P0.1/RXD Interrupt Flag P0IFG.1 (located in IFG1.3, initial state is reset)
- P0.0 Interrupt Enable P0IE.0 (located in IE1.2, initial state is reset)
- P0.1/RXD Interrupt Enable P0IE.1 (located in IE1.3, initial state is reset)
- P0.0 Interrupt Edge Select (located in P0IES.0, initial state is reset)
- P0.1/RXD Interrupt Edge Select (located in P0IES.1, initial state is reset)

Both interrupt flags are single source interrupt flags and are automatically reset when the processor system serves them. The enable bits and edge select bits remain unchanged.

The interrupt control bits of the remaining six I/O signals P0.2 to P0.7 are located in the I/O address frame. Each signal uses three bits that define reaction to interrupt events:
- interrupt flag, P0IFG.2 to P0IFG.7
- interrupt enable bit, P0IE.2 to P0IE.7
- interrupt edge select bit, P0IES.2 to P0IES.7

The interrupt flags P0IFG.2 to P0IFG.7 are part of a multiple source interrupt request. Any interrupt event on one or more pins of P0.2 to P0.7 will request an interrupt when two conditions are met: the appropriate individual bit P0IE.x ($2 \le x \le 7$) is set and the general interrupt enable bit GIE is set. The six interrupt sources use the same interrupt vector. Since the interrupts share the same interrupt vector, interrupt flags P0.2 to P0.7 are not automatically reset.

The software of the interrupt service routine handles the detection of the source, and also resets the appropriate flag when it is serviced.

Note: Multiple Source interrupt flags P0IFG.2 to P0IFG.7

The interrupt flags P0IFG.2 to P0IFG.7 remain set when an interrupt request has been accepted and serviced. This is mandatory, because it is a multiple source interrupt. Each flag that was served should be reset within its interrupt service routine.

8.2 General Ports P1, P2

The general port P1 and port P2 incorporates all the functions to individually select the function of each pin and to use each signal as an interrupt source.
The seven registers are used to control the Port's I/O pins.
The general module registers are mapped into the lower peripheral file address range where all byte modules are located. The register should be accessed with byte instructions, using absolute address mode.

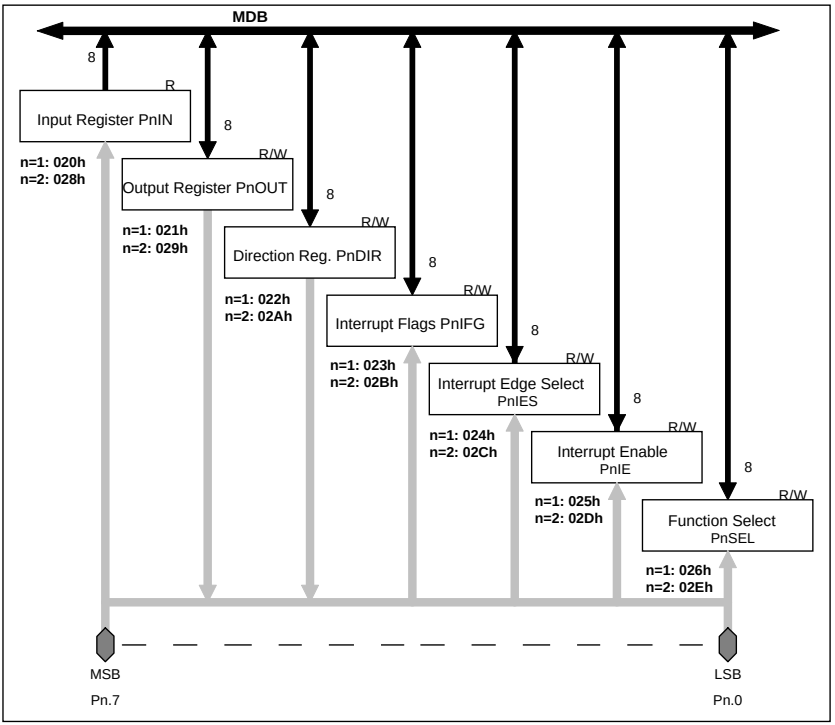

Figure 8.6: Port P1, Port P2 Configuration

8.2.1 Port P1, Port P2 Control Registers

The port P1 and port P2 are connected to the processor core via the 8-bit MDB structure and MAB. They should be accessed via byte instructions.

The seven control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently:
- Any combination of input, output and interrupt condition is possible.
- Interrupt processing of external events is fully implemented for all eight bits of the port P1 and port P2.

The seven registers for port P1 and the seven registers for port P2 are:

Register	short form	Register type	Address	Initial State
• Input register:	P1IN	read only	020h	-----
• Output register:	P1OUT	read/write	021h	unchanged
• Direction register:	P1DIR	read/write	022h	reset
• Interrupt Flags:	P1IFG	read/write	023h	reset
• Interrupt Edge Select:	P1IES	read/write	024h	unchanged
• Interrupt Enable:	P1IE	read/write	025h	reset
• Function Select reg.:	P1SEL	read/write	026h	reset
• Input register:	P2IN	read only	028h	-----
• Output register:	P2OUT	read/write	029h	unchanged
• Direction register:	P2DIR	read/write	02Ah	reset
• Interrupt Flags:	P2IFG	read/write	02Bh	reset
• Interrupt Edge Select:	P2IES	read/write	02Ch	unchanged
• Interrupt Enable:	P2IE	read/write	02Dh	reset
• Function Select reg.:	P2SEL	read/write	02Eh	reset

All these registers contain eight bits. The registers should be accessed with byte instructions and use absolute address mode.

Input Registers P1IN, P2IN
Both input registers are read-only registers to scan the signals at the I/O pins. The direction of the pin should be selected for input.

> **Note: Writing to read only registers P1IN, P2IN**
>
> Writing to this read-only register results in an increased current consumption as long as the write is active.

Output Registers P1OUT, P2OUT
Each output register shows the information of the output buffer, an eight bit register that contains the information output at the I/O pins if used as outputs. The output buffer can be modified by all instructions that write to a destination. If read, the contents of the output buffer is read independently of the direction. A direction change does not modify the output buffer contents.

Direction Registers P1DIR, P2DIR
Each register contains eight independent bits that define the direction of the I/O pin. All bits are reset by PUC:

Bit = 0: The I/O pin is switched to input direction
Bit = 1: The I/O pin is switched to output direction

Interrupt Flags P1IFG, P2IFG
Each register contains eight flags that contain information if an interrupt is pending or not - according to the corresponding I/O pin:

Bit = 0: No interrupt is pending
Bit = 1: An interrupt is pending due to a transition at the I/O pin. Manipulation on P1OUT and P1DIR as well as P2OUT and P2DIR can also set bits of P1IFG or P2IFG.

Writing a zero to an Interrupt Flag resets it.

Note: Interrupt Flags P1FLG02...7, P2FLG02...7

Each group of the Interrupt Flags P1FLG.0 to P1FLG.7 and P2FLG.0 to P2FLG.7 use only one interrupt vector: both are multiple source interrupt vectors. The interrupt flags P1IFG.0 to P1IFG.7 and P2FLG.0 to P2FLG.7 are not reset automatically when any interrupt from these events is served. The software decides which event will be served and should reset the appropriate flag.

Any external interrupt event should be as long as 1.5 times MCLK or longer, to ensure that it is accepted and the corresponding interrupt flag is set.

Interrupt Edge Select P1IES, P2IES
Each register contains a bit for e corresponding ach I/O pin that selects which transition triggers the interrupt flag. All eight bits according to pin P1.0 to P1.7 and to pin P2.0 to P2.7 are located in these registers. The bits have the following meaning:

Bit = 0: The interrupt flag is set with LO/HI transition
Bit = 1: The interrupt flag is set with HI/LO transition

Note: Change of P1IES, P2IES bit(s)

Changing P1IES, P2IES bit(s) may result in setting the associated interrupt flags:

Bit PnIES.x	PnIN.x	PnIFG.x
0 > 1	0	unchanged
0 > 1	1	may be set
1 > 0	0	may be set
1 > 0	1	unchanged

Interrupt Enable P1IE, P2IE

Each register contains a bit for all eight I/O pins to enable interrupt request on an interrupt event. Each of the eight bits corresponding to pin P1.0 to P1.7 and P2.0 to P2.7 are located in the P1IE and P2IE registers.

The bits have the following meanings:

Bit = 0: The interrupt request is disabled
Bit = 1: The interrupt request is enabled

Note: Port P1, Port P2 interrupt sensitivity

Only transitions, not static levels, cause interrupts.

The interrupt routine must reset all Interrupt Flags, since they follow the multiple interrupt bit scheme of the MSP430 family.

If an Interrupt Flag is still set (because the transition occurred during the interrupt routine) when the *RETI* instruction is executed, an interrupt occurs again after *RETI* is completed. This ensures, that each transition is seen by the software.

Function Select Registers P1SEL, P2SEL

Each register contains eight independent bits that define the functions that access the I/O pin. The port function or a defined module function puts data to the pin, or gets data from the pin. All bits are reset by PUC:

Bit = 0: Port function - output or input data are defined by the port module
Bit = 1: Module function - output or input data are defined by a module not by the port module

Note: Function Select with P1SEL, P2SEL

The interrupt edge select circuitry is disabled if control bit PnSEL.x is set. The input signal will not alter the interrupt flag.
The interrupt edge select and the interrupt flag operates with their full performance when the function select control bit PnSEL is reset.

8.2.2 Port P1, Port P2 Schematic

The pin logic of each individual signal of port P1 and port P2 is identical. Each bit can be read and written.

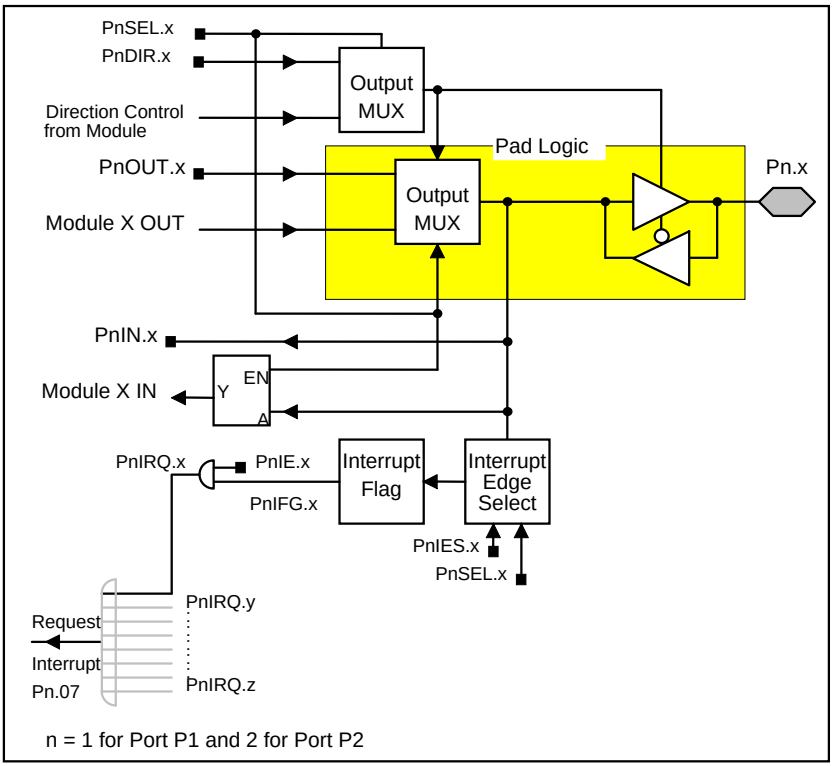

Figure 8.7: Schematic of one bit in Port P1, P2

Module X IN function

The input signal fed to a peripheral module follows the input when the module's function is selected - PnSEL.x = 1. It will be halted continuously at the last level of the input that was passed to the module before the control bit PnSEL.x was reset. Setting the control bit from reset state can alter the signal to the module, when the halted level and the actual level at the input are different.

8.2.3 Port P1, P2 interrupt control functions

Port P1 and port P2 use eight bits for interrupt flags, eight bits for interrupt enable, eight bits to select the effective edge of an interrupt event and one interrupt vector address for port P1 and one interrupt vector address for port P2.

All of the interrupt control bits are located in the I/O address frame. Each signal uses three bits that define reaction to interrupt events:

- interrupt flag, P1IFG.0 to P1IFG.7 and P2IFG.0 to P2IFG.7
- interrupt enable bit, P1IE.0 to P1IE.7 and P2IE.0 to P2IE.7
- interrupt edge select bit, P1IES.0 to P1IES.7 and P2IES.0 to P2IES.7

The interrupt flags P1IFG.0 to P1IFG.7 and P2IFG.0 to P2IFG.7 are part of a multiple source interrupt request. Any interrupt event on one or more pins P1.0 to P1.7 or P2.0 to P2.7 will request an interrupt when two conditions are met, the appropriate individual bit PnIE.x ($0 \leq x \leq 7$) is set, and the general interrupt enable bit GIE is set. The eight interrupt sources use the same interrupt vector. Since the interrupt shares the same interrupt vector, none of the interrupt flags P1.0 to P1.7 or P2.0 to P2.7 is reset automatically.

The software of the interrupt service routine must handle the detection of the source and also resets the appropriate flag when it is serviced.

Note: Multiple Source interrupt flags P1IFG.0 to P1IFG.7, P2IFG.0 to P2IFG.7

The interrupt flags P1IFG.0 to P1IFG.7 and P2IFG.0 to P2IFG.7 remain set when an interrupt request has been accepted and serviced. This is mandatory because it is a multiple source interrupt. Each flag that was served should be reset within its interrupt service routine.

8.3 General Ports P3, P4

The general port P3 and port P4 are identical. They incorporate all the functions to individually select the function of each pin. Each pin can be selected to operate with the port function, or to operate under control of another internal peripheral module.
Four registers control each of the two ports P3 and P4.
The general module registers are mapped into the lower peripheral file address range where all byte modules are located. The register should be accessed with byte instructions, using absolute address mode.

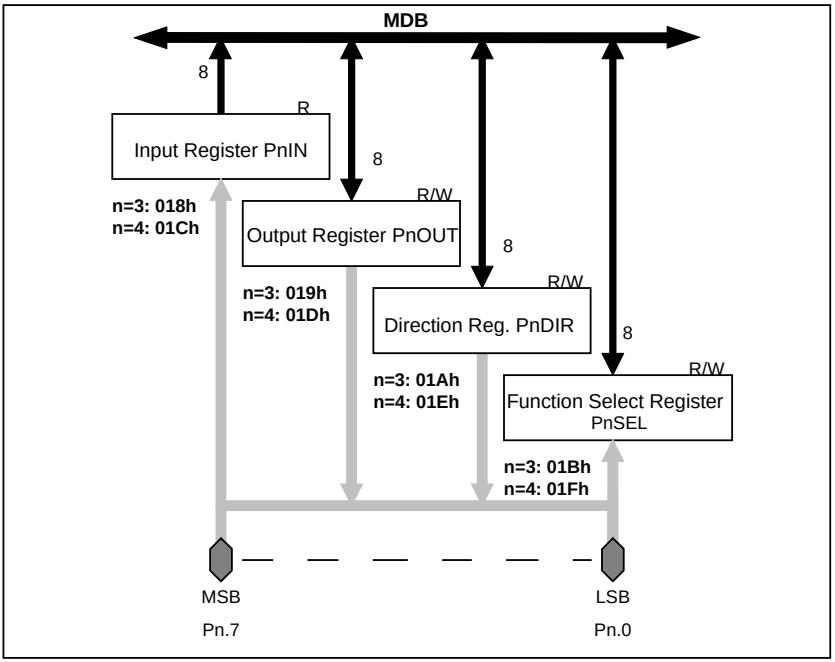

Figure 8.8: Port P3, Port P4 Configuration

8.3.1 Port P3, Port P4 Control Registers

The port P3 and port P4 are connected to the processor core via the 8-bit MDB structure and MAB. They should be accessed via byte instructions using absolute address mode.

The four control registers of each port give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently:
- Any combination of input is possible.
- Any combination of port or module function is possible.

The four registers for each port are:

Register	short form	Register type	Address	Initial State
• Input register:	P3IN	read only	018h	-----
• Output register:	P3OUT	read/write	019h	unchanged
• Direction register:	P3DIR	read/write	01Ah	reset
• Port Select register:	P3SEL	read/write	01Bh	reset
• Input register:	P4IN	read only	01Ch	-----
• Output register:	P4OUT	read/write	01Dh	unchanged
• Direction register:	P4DIR	read/write	01Eh	reset
• Port Select register:	P4SEL	read/write	01Fh	reset

All these registers contain eight bits and should be accessed with byte instructions.

Input Register P3IN, P4IN
The input registers are read-only registers to scan the signals at the I/O pins. The direction of the pin and the port function should be selected for input

> **Note: Writing to read only register P3IN, P4IN**
>
> Writing to this read only registers results in an increased current consumption, as long as the write is active.

Output Registers P3OUT, P4OUT
The output registers P3OUT and P4OUT show the information of the output buffer, each an eight bit register that contains the output information at the I/O pins if used as outputs. The output buffer can be modified by all instructions that write to a destination. If read, the contents of the output buffer are read independently of the direction. A direction change does not modify the output buffer contents.

Direction Registers P3DIR, P4DIR
Each register contains eight independent bits that define the direction of the I/O pin. All bits are reset by PUC:

Bit = 0: The I/O pin is switched to input direction
Bit = 1: The I/O pin is switched to output direction

Function Select Register P3SEL, P4SEL
Each register contains eight independent bits that define the functions that access the I/O pin. The port function or a defined module function puts data to the pin, or gets data from the pin. All bits are reset by PUC:

Bit = 0: Port function - output or input data are defined by the port module

Bit = 1: Module function - output or input data are defined by a module not by the port module

8.3.2 Port P3, Port P4 Schematic

The pin logic of each individual signal of port P3 and port P4 is defined in the specific device configuration. In these device specifications, the function - purely digital port or port function shared with module functions - are defined.
Pins which are used only with digital port function are exclusively controlled by the bits in the corresponding four port registers.
Pins which are used with digital port and module function are controlled by

- the port control bits, when the corresponding select bit PnSEL.x is reset
- the module control bits, when the corresponding select bit PnSEL.x is set

All eight port signal can be configured by the hardware individually to be:

- port pin only
- module function pin only
- software configurable for port or module function

The specific realization is described in the device data sheet.

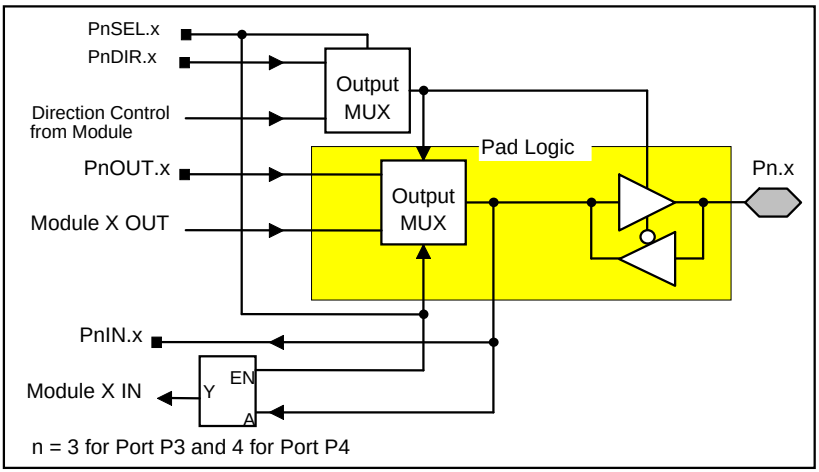

Figure 8.9: Schematic of bits P3.x/P4.x

Module XIN function

The input signal fed to a peripheral module follows the input when the module's function is selected - PnSEL.x = 1. It will be halted continuously at the last level of the input that was passed to the module before the control bit PnSEL.x was reset. Setting the control bit from reset state can alter the signal to the module when halted level and actual level at the input are different.

8.4 LCD Ports

The LCD ports can be selected either to drive a liquid crystal display, or to act as digital outputs driving static output signals. The control of a liquid crystal display uses common and segment output stages to drive the analog signals needed for multiplex rates of 2Mux and higher.

LCD outputs

The LCD outputs use transmission gates to transfer the analog voltage to the output pin, when they are used to drive liquid crystal displays. Groups of LCD outputs can be configured by software to operate as digital outputs.

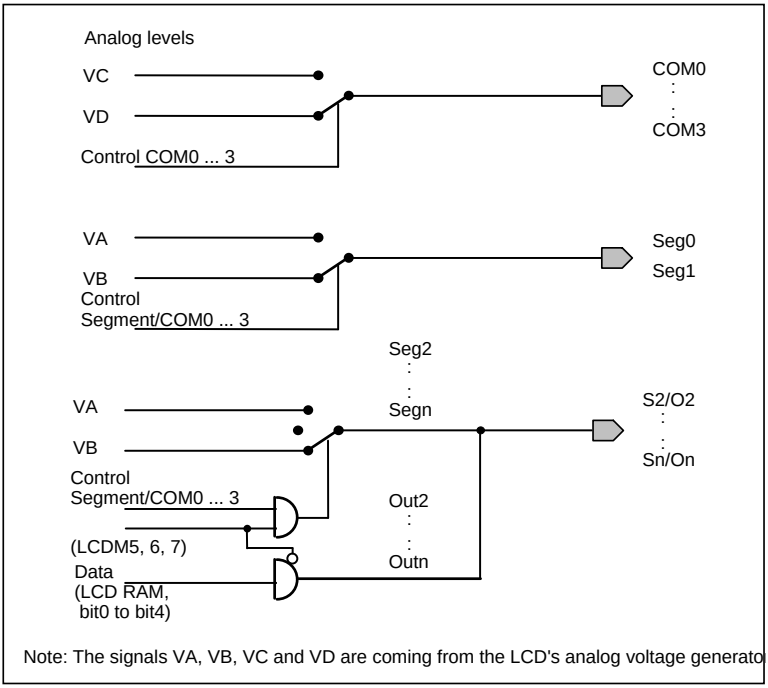

Figure 8.10: Schematic of LCD

Three bits in the LCD control register LCDM5, LCDM6 and LCDM7 control the function of these groups of signals. For more information on control of these outputs, see LCD description.

8.5 LCD Port - Timer/Port Comparator

The comparator associated with the Timer/Port module is shared typically with one segment line. The segment line function is selected for this pin after PUC signal was active. The comparator input is selected when the CPON bit - located in the Timer/Port module - is set the first time. It remains set as long as it is not reset by PUC.

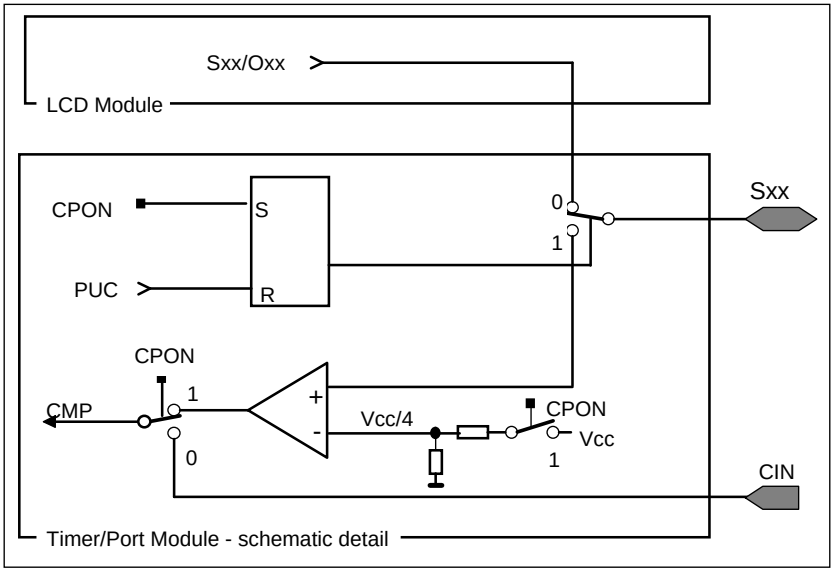

Figure 8.11: Schematic of LCD pin - Timer/Port Comparator