16 Miscellaneous Modules

16.1 Crystal Oscillator

All elements for crystal operation are integrated into the MSP430 - no additional external components are necessary for operation. Since the oscillator is designed for ultra-low power dissipation the PWB layout should provide short connections between the crystal and the MSP430 device.

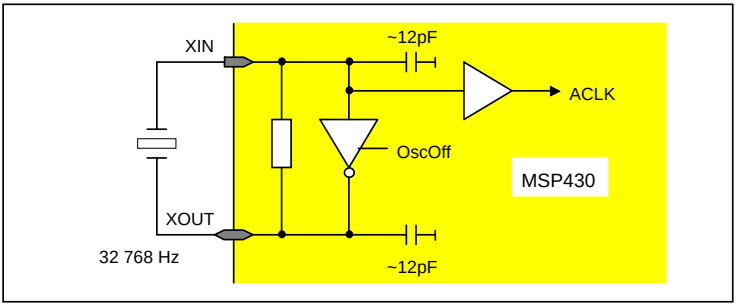

Figure 16.1: Crystal Oscillator schematic

When OscOff mode is selected the ACLK signal is held to high.

16.2 Power-on Circuitry

The power-on circuitry is part of the system reset scheme, and consists of two parts: the power-on reset detection, and the power-on reset delay. The output of the POR delay is fed into the POR latch and the PUC latch to set both latches, in order to supply the system with the reset condition.

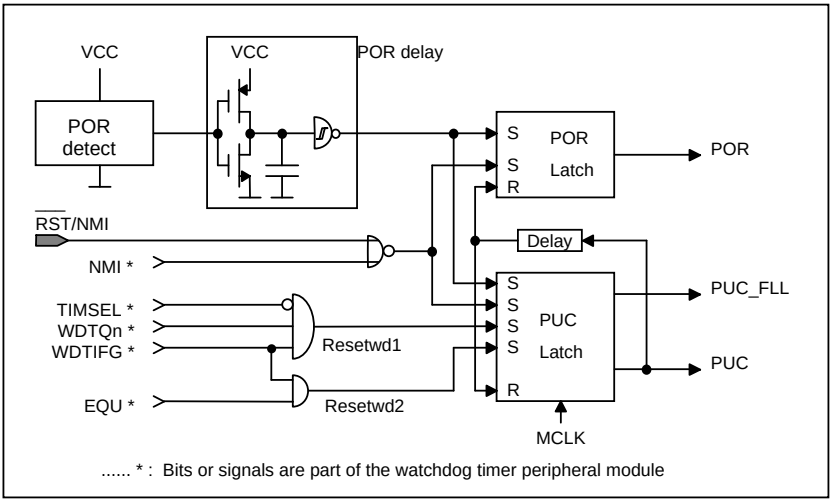

Figure 16.2: Power-on reset and Power-up clear schematic

When the VCC supply provides a fast VCC rise time, the POR delay gives enough active time on the POR signal to allow it to initialize the circuit correctly after power-up.

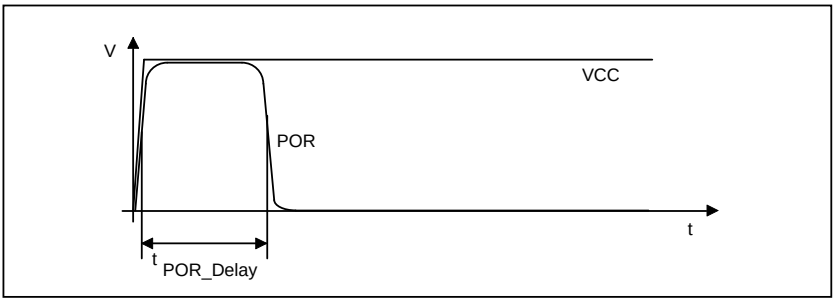

Figure 16.3: Power-on reset timing on fast VCC rise time

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When the VCC supply provides a 'slow' VCC rise condition the POR detect defines the POR signal to allow it to initialize the circuit correctly after power-up.

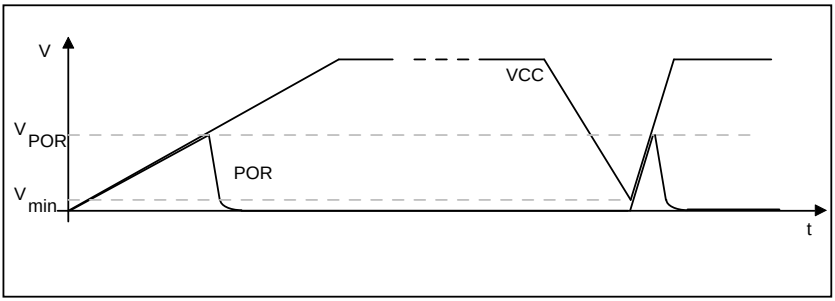

Figure 16.4: Power-on reset timing on slow VCC rise time

The supply voltage VCC should fall below V_{min} to ensure another POR signal occurs with the next increase in supply voltage. If V_{CC} does not fall below V_{min} a POR will not be generated and power-up conditions will not be set properly.

16.3 Crystal Buffer Output

The frequency of the buffer output is selected via the control register CBCTL.

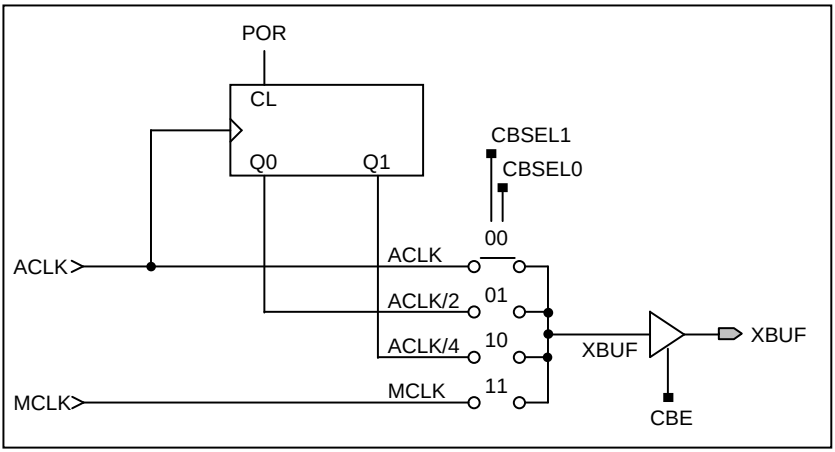

Figure 16.5: Schematic of Crystal Buffer

The control register CBCTL of the clock buffer output peripheral has bits that control the frequency applied to pin XBUF, and one bit that controls the 3-state condition of the output buffer.

The divider runs with the minimum of logic necessary for correct operation. For example, it is halted when ACLK or MCLK is selected or if the CBE bit is set.

The three bits in the control register CBSEL1, CBSEL0 and CBE are reset with POR signal. The POR signal is active either during switching on V_{CC} or when $\overline{\text{RST/NMI}}$ -pin is tied to V_{SS} when reset function is selected.

CBCTL
053h

---	---	---	---	---	CBSEL 1	CBSEL 0	CBE
					w-(0)	w-(0)	w-(0)

Bit 0: The bit CBE controls the 3-state condition of the output buffer.
CBE = 1: Output buffer enabled
CBE = 0: Output buffer disabled
During power-on reset (POR) the output buffer is always disabled. External components are not supplied with the selected frequency.

Bit 1,2: The bits CBSEL1 and CBSEL0 select the frequency that can be put onto output pin XBUF.

CBSEL1	CBSEL0	XBUF1	
0	0	ACLK	← State after POR
0	1	ACLK/2	
1	0	ACLK/4	
1	1	MCLK	

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