New Logic Family Achieves Highest Speeds at Lower Voltages

by Stephen Nolan and Ji Park, Texas Instruments

Workstations, servers, and other high-performance systems are reaching new heights in innovation daily. As these products improve, bus- and memory-interface devices must keep pace and must advance to greater speeds as well. Moreover, these systems require that this increased speed be coupled with lower power consumption. This imperative usually means a lower voltage node. Also to function as viable solutions, these logic devices must reach these faster and faster speeds without sacrificing signal integrity.

Texas Instruments' new logic family, the AVC (Advanced Very-low-voltage CMOS) family, delivers both high speed and low power without reducing signal quality. AVC logic follows on the heels of TI's ALVC (Advanced Low Voltage CMOS) logic, which helped engineers make the transition from 5-V to 3.3-V designs beginning in 1994. Many designs are now migrating from 3.3-V to 2.5-V, creating new design challenges. Complicating this transition is the industry's appetite for higher system speeds, which has driven bus speeds above the 125-MHz mark (Figure 1). The AVC logic family is the first logic family in the industry with propagation delays of less than two nanoseconds (2 ns).

High-speed logic usually generates significant undershoot and overshoot noise from the very fast signal transitions. Series damping resistors are sometimes used to reduce electrical noise; but resistors, whether they are internal or external to the logic, also slow the speed of the signals through the circuitry. The AVC family does not require series damping resistors to reduce electrical noise (Figure 2).

TI has developed a unique innovation called Dynamic Output Control (DOC™) (patent pending), which gives AVC logic "the best of both worlds." Specifically, AVC logic achieves very high signaling speeds because the circuitry behaves as though there were no resistors in the output when a signal transition is taking place. Then, as the signal transition nears completion, circuitry is automatically activated that behaves as though there were series damping resistors on the output. This capability dramatically

minimizes the signal undershoot or overshoot and effectively muffles electrical noise.

In addition to high-speed and low electrical noise, AVC consumes little power and is easy to design into a mixed-voltage system. Although AVC is very low power with its optimization for 2.5-V systems, it remains compatible with 3.3-V or even 1.8-V components as well. In fact, AVC is operational from 1.65 V to 3.6 V. Moreover, AVC logic can save battery life since it has a feature that supports partial power off--thus allowing the power to be turned off to portions of a system when those sections are not in use.

The AVC family is over-voltage tolerant at both the inputs and the outputs--a feature which helps the engineer who is faced with a mixed voltage mode design. For example, if a design calls for interfacing a 2.5-V memory controller with 3.3-V memories, all the designer needs to do is place an AVC transceiver in between the memory controller and the memories. The AVC device, powered at 2.5 V, will provide reliable bi-directional data communication between the devices at these two voltage nodes. The data from the 3.3-V memories are accepted at the inputs of the AVC transceiver without any problems, since the transceiver's inputs are over-voltage tolerant. Also, an AVC driver or register device, powered at 1.8 V, can be used to provide uni-directional data communication from devices at the 3.3-V or the 2.5-V nodes to devices at 1.8 V.

Dynamic Output Control (DOC)

The way the AVC family's DOC circuitry handles high-speed signals is similar to the way a race car driver negotiates an oval track. On the straight-aways, the driver can accelerate to maximum speed. But, as he approaches a curve in the track, the driver must slow down or risk losing control of the car. In much the same way, DOC circuitry (Figure 3) allows the signaling to accelerate to its maximum speed during the transition from a low to a high state (or from a high to a low). Then, in much the same way that a race car driver eases off the accelerator as he negotiates a curve, the DOC circuitry reduces the power of the electrical signal when the transition nears completion. This reduction minimizes overshoot and undershoot noise that would otherwise be generated by a high-speed signal transition. Specifically, DOC lowers the output impedance of the circuitry at the beginning of a signal transition to drive the load at high speeds. Then, as the end of transition is near, DOC

automatically raises the impedance to roll-off the signal and to reduce noise.

(figure 4)

The DOC effectively consists of two parallel drivers and an impedance control circuit (ZCC) that monitors the output signal. When the impedance control circuit senses that more current is needed, the outputs of both the parallel drivers are enabled, thereby reducing the output impedance. As the signal passes through the threshold during a transition, the impedance control circuit disables the output of one of the drivers, thereby increasing the output impedance. Obviously, the driver that is disabled does not contribute any additional drive current or loading to the output.

Bus Hold™

(figure 5)

The bus hold feature was also included in the AVC family of logic devices. Bus hold helps solve the problem of floating inputs and eliminates the need for pull-up or pull-down resistors. With the totem-pole structure that characterizes the inputs of CMOS devices, the input must be held as close to VCC or GND rails as possible. Precautions should be taken to prevent the input voltage from floating near the threshold voltage because this eventuality would bias both input transistors on and would create undesirably high ICC currents at the VCC pin of the device. One possible method would be to use pull-up or pull-down resistors, but these are costly and take up additional circuit-board area. An alternative solution is to use devices in the AVC family that utilize the optional bus-hold circuit at the inputs. AVC devices with bus-hold circuitry are designated AVCH.

The bus-hold circuit consists of two series inverters with the output fed back to the input through a resistor. This arrangement provides a weak positive feedback by sinking or sourcing current to the input node. The bus-hold circuit consists of two series inverters with the output fed back to the input through a resistor. This arrangement provides a weak positive feedback

by sinking or sourcing current to the input node. The bus-hold cell holds the input at its last known valid logic state until this state is forcibly changed by a driving circuit.

A Full Family of Logic

A comprehensive selection of AVC devices is planned for introduction over the next two years. The AVC product portfolio will be comprised of gate, octal, Widebus™, and Widebus+™ logic devices. A complete selection of different device types such as bus drivers and transceivers, buffers, flip-flops, latches, and address drivers will eventually find their way into the AVC family. Samples of the first four members of the AVC logic family should be available from Texas Instruments and its authorized distributors in the fourth quarter of 1998. Part numbers and anticipated resale pricing in quantities of 1000 are as follows: AVC16244 16-bit buffer $2.92, AVC16245 16-bit transceiver $2.92, AVC16373 16-bit D-type transparent latch $2.92, and AVC16374 16-bit D-type flip-flop $2.92. Military versions of selected AVC functions are also planned.

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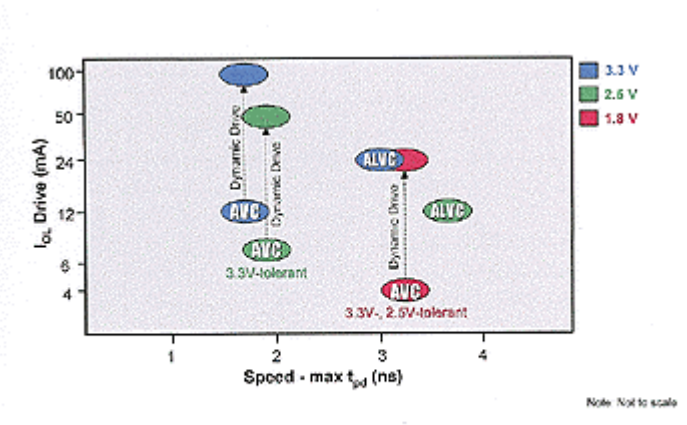
About the Authors

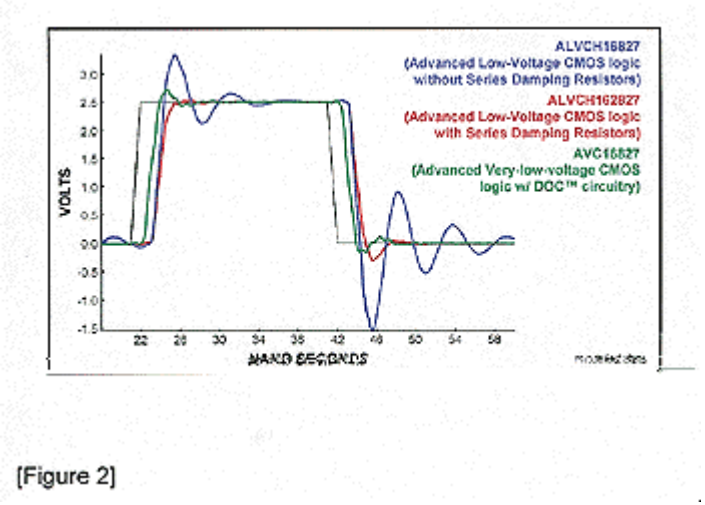
Stephen Nolan is the senior applications engineer for Texas Instruments' CBT and CBTLV bus switches and the AVC (Advanced Very-low-voltage CMOS) logic family. Nolan had previously worked in TI's BiPolar wafer fabrication family as a photo lithography engineer. He has a BS in electronics engineering technology and a MS in electronics engineering technology from Southeastern Oklahoma State University.

Ji Park's Advanced Computing Solutions team at TI is responsible for the strategic development of advanced logic devices for PCs, workstations, and servers. Park received a BSEE from the University of Texas.



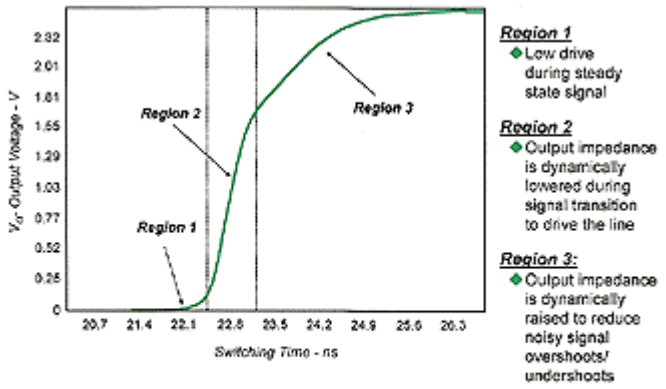
[Figure 1]

Figure 1. AVC Performance Characteristics



[Figure 2]

Figure 2. AVC Noise Performance versus Other High-Speed, Low-Voltage Logic Solutions



[Figure 3]

Figure 3. The Three Stages of Dynamic Output Control (DOC™)

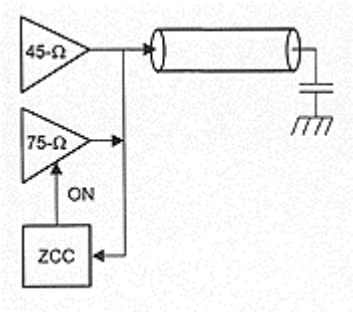


Figure 4 DOC Circuitry

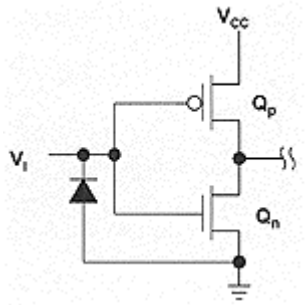


Figure 5 Bus Hold Circuit