Control Loop Modeling of Switching Power Supplies

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Abstract

This paper presents techniques to assist the power supply designer in accurately modeling and designing the control loop of a switchmode DC/DC power supply. The three major components of the power supply control loop (i.e., the power stage, the pulse width modulator and the error amplifier) are presented with power stage modeling being the focus of this presentation. The power stage is modeled using the PWM Switch model, which greatly simplifies the analysis over state-space averaging methods. Voltage mode pulse-width-modulation is presented.

Introduction

There are many facets to the analysis and design of a switching power supply. The power supply designer must have a good understanding of basic analog circuit theory, a small but ever increasing grasp of digital circuits, at least a passing comprehension of electromagnetic fundamentals and a proficient knowledge of control system concepts. This paper deals with modeling the frequency response characteristics of a switching power supply control loop.

A regulated switching power supply control loop consists of three major components; the power stage, the reference voltage/error-amplifier combination, and the pulse-width-modulator. Figure 1 is a simple block diagram of a switching power supply showing these components. The power stage performs basic voltage conversion. Modeling the power stage presents the fundamental challenge to the power supply designer. A relatively new technique involves modeling only the switching elements of the power stage. An equivalent circuit for these elements is derived and is called the *PWM Switch Model*. This approach is presented here. Once an accurate and easy-to-use model for the power stage is obtained, the power supply designer can design the reference voltage/error-amplifier circuit so that a stable and fast-responding control loop results. The reference voltage and error-amplifier provide a signal which, roughly speaking, indicates the closeness of the output voltage to the desired value. Modeling this part of the control loop is easy because they are linear circuits and are easily represented mathematically. Finally, the pulse-width-modulator converts the analog output signal of the error-amplifier to a digital pulse train that is used by the power stage to produce the output voltage. The model for the pulse-width-modulator is relatively straightforward. It can be said that a regulated switching power supply has all the components of a classical control system: a plant, a reference input, and a feedback network.

The techniques presented here can be used to analyze many of the various types of regulated switching power supplies. In order to limit the scope of this paper, the discussion will be limited to DC/DC converters.

Figure 1. Power Supply Control Loop Components

Referring to Figure 1, let us qualitatively explain the operation of the control loop. The error-amplifier has two inputs; the reference voltage and the output voltage. The amplifier output, called V_E, is the difference in these two signals. Thus, if the power supply output voltage is too low, the error-amplifier output will tend to increase. An increase in V_E causes a corresponding increase in duty cycle by the action of the pulse-width-modulator. This increase in duty cycle applied to the power stage causes an increase in output voltage.

Power Stage Modeling

There are three commonly used power stage topologies: buck, boost, and buck-boost. Each converter has unique characteristics that make it desirable for particular applications. For example, the buck converter can only produce an output voltage that is lower than the input voltage while the boost converter only produces an output voltage that is higher than its input. As shown in Figure 1, the power stage has two inputs: the input voltage and the duty cycle. The duty cycle is the control input, i.e., this input is a logic signal which controls the switching action of the power stage and hence the output voltage. Most power stages have a non-linear voltage gain versus duty cycle. This non-linear behavior is a result of the converter switching action. To illustrate this nonlinearity, a graph of the steady-state voltage gain for a boost converter as a function of steady-state duty cycle, D, is shown in Figure 2.

Figure 2. Boost Power Stage Gain vs. Duty Cycle

The basic goal behind modeling power stages is for the model to represent the operation at a given operating point and to be linear around the operating point. We want linearity so that we can apply the many analysis tools available for linear systems. Referring again to Figure 2, if we choose the operating point of $D = 0.7$, a straight line can be constructed that is tangent to the original curve at the point where $D = 0.7$. This is an illustration of linearization about an operating point. Qualitatively, one can see that if the variations in duty cycle are kept small, a linear model accurately represents the non-linear behavior of the power stage being analyzed.

The non-linear characteristics are a result of the switching action of the power stage switching components, Q1 and CR1. It was observed in reference [2] that the only non-linear components in a power stage are the switching devices; the remainder of the circuit consists of linear elements. It was also shown in reference [2] that a model of the non-linear components could be derived by averaging these components over one switching cycle. The model is then substituted into the original circuit for analysis of the complete power stage. Thus, a model of the switching devices is given and is called the *PWM Switch* model.

PWM Switch Model – Continuous Conduction Mode

To start modeling the power stage, we begin with the derivation of the PWM Switch model in continuous conduction mode (CCM). CCM is characterized by the inductor current never reaching zero during any portion of the switching cycle. We focus on the CCM Buck converter shown in Figure 3. The strategy is to average the switching waveforms over one switching cycle and produce an equivalent circuit for substitution into the remainder of the power stage. The waveforms that are averaged are the voltage across CR1, v_{cp}, and the current in Q1, i_a. The waveforms are shown in Figure 4.

Figure 3. Buck Converter Power Stage

Referring to the figure above, the resistor, R, represents the load seen by the power supply output. The power transistor, Q1, and the catch diode, CR1, are drawn inside a dashed-line box. These are the components that will be replaced by the PWM Switch equivalent circuit. The terminals labeled a, p, and c will be used for terminal labels of the PWM Switch model.

Figure 4. Buck Converter Waveforms

Referring to the waveforms in Figure 4, regarded as instantaneous quantities, the following relationships are obviously true:

$$i_a(t) = \begin{cases} i_c(t) & during \quad d\,T_s \\ 0 & during \quad d'\,T_s \end{cases}$$

$$v_{cp}(t) = \begin{cases} v_{ap}(t) & during \quad d\,T_s \\ 0 & during \quad d'\,T_s \end{cases}$$

where: $i_a(t)$ and $i_c(t)$ are the instantaneous currents during a switching cycle and

$v_{cp}(t)$ and $v_{ap}(t)$ are the instantaneous voltages between the indicated terminals.

If we take the average over one switching cycle of the above quantities, we get:

$$\langle i_a \rangle = d * \langle i_c \rangle \tag{1}$$

$$\langle v_{cp} \rangle = d * \langle v_{ap} \rangle \tag{2}$$

where the brackets indicate averaged quantities.

Now, we can implement the above averaged equations in a simple circuit using dependent sources:

Figure 5. Averaged (nonlinear) CCM PWM Switch Model

The above model is one form of the PWM switch model. However, in this form it is not very useful. We now need to perform perturbation and linearization and then the PWM switch model will be in the desired form, i.e. linearized about a given operating point.

The main idea of perturbation and linearization is assuming an operating point and introducing small variations about that operating point. For example, we assume that the duty ratio is fixed at $d = D$ (capital letters indicate steady-state, or DC quantities while lower case letters are for time-varying, or AC quantities). Then a small variation, $\hat{d}$, is added to the duty cycle so that the complete expression for the duty cycle becomes: $d(t) = D + \hat{d}(t)$. Note that the ^ (hat) above the quantities represents perturbed or small AC quantities. Now we apply the above process to equations (1) and (2) to obtain:

$$I_a + \hat{i}_a = \left(D + \hat{d}\right) * \left(I_c + \hat{i}_c\right) = D * I_c + D * \hat{i}_c + \hat{d} * I_c + \hat{d} * \hat{i}_c$$

$$V_{cp} + \hat{v}_{cp} = \left(D + \hat{d}\right) * \left(V_{ap} + \hat{v}_{ap}\right) = D * V_{ap} + D * \hat{v}_{ap} + \hat{d} * V_{ap} + \hat{d} * \hat{v}_{ap}$$

Now, we separate steady-state quantities from AC quantities. We also drop products of AC quantities because the variations are assumed to be small and products of two small quantities are assumed to be negligible. We arrive at the steady-state and AC relationships or in other words, the DC and small signal model:

$I_a = D * I_c$	Steady-State
$\hat{i}_a = D * \hat{i}_c + \hat{d} * I_c$	AC
$V_{cp} = D * V_{ap}$	Steady-State
$\hat{v}_{cp} = D * \hat{v}_{ap} + \hat{d} * V_{ap}$	AC

In order to implement the above equations into a simple circuit, first notice that the two steady-state relationships can be represented by an ideal (independent of frequency) transformer with turns ratio equal to *D*. Including the AC quantities is straightforward after reflecting all dependent sources to the primary side of the ideal transformer. The DC and small-signal model of the PWM Switch is shown in Figure 6. It can easily be verified that the model below satisfies the above four equations.

Figure 6. DC and Small Signal CCM PWM Switch Model

This model can now be substituted for Q1 and CR1 in the buck converter to obtain a model suitable for DC or AC analysis and is shown below.

Figure 7. CCM Buck Converter Model

Now, an explanation of the terminal naming convention is in order. The terminal named *a* is for *active*; it is the terminal connected to the active switch. Similarly, *p* is for *passive* and is the terminal of the passive switch. Lastly, *c* is for *common* and is the terminal that is common to both the active and passive switches. Interestingly enough, the three commonly used power stage topologies contain active and passive switches and the above terminal definitions can be also applied. More interestingly, it is true that substituting the PWM Switch model into other power stage topologies also produces a valid model. To use the PWM Switch model in other power stages, just substitute the model shown in Figure 6 into the power stage in the appropriate orientation.

To illustrate how simple power stage analysis becomes with the PWM switch model, consider the following. For DC analysis, $\hat{d}$ is zero, L1 is a short and C is an open. Then by inspection one can see $V_I * D = V_O$. We also see that $V_{ap} = V_I$. Thus, knowing the input voltage and output voltage, *D* is easily calculated. For AC analysis, the following transfer functions can be calculated: Open-Loop Line-to-Output, Open-Loop Input Impedance, Open-Loop Output Impedance, and Open-Loop Control-to-Output. The Control-to-Output, or duty-cycle-to-output, is the transfer function preferred for control loop analysis. To determine this transfer function, first, use the results from the DC analysis for operating point information. In particular, $V_{ap} = V_I$. Then set the input voltage equal to zero because we only want the AC component of the transfer function. Finally, writing the equations gives:

$$-\frac{V_{ap}}{D} * \hat{d} + \frac{\hat{v}_{cp}}{D} = 0 \Rightarrow \frac{\hat{v}_{cp}}{\hat{d}} = V_{ap} = V_I$$

$$\frac{\hat{v}_O}{\hat{v}_{cp}} = \frac{Z_{RC}(s)}{Z_{RC}(s) + Z_L(s)} \quad \text{by voltage division}$$

where

$$Z_{RC}(s) = \frac{R}{1 + s * R * C} \quad \text{(parallel combination of output R and output C)}$$

$$Z_L(s) = s * L$$

So, after simplifying, the desired transfer function is:

$$\frac{\hat{v}_O}{\hat{d}}(s) = \frac{\hat{v}_O}{\hat{v}_{cp}}(s) * \frac{\hat{v}_{cp}}{\hat{d}}(s) = V_I * \frac{1}{1 + s * \frac{L}{R} + s^2 * L * C}$$

which is exactly what is obtained by other modeling procedures.

PWM Switch Model – Discontinuous Conduction Mode

We now continue our discussion of modeling the power stage when it is operating in discontinuous conduction mode (DCM). This mode is quite different from continuous conduction mode just covered. We begin with the derivation of the PWM Switch model for DCM focusing on the Buck-Boost topology shown in Figure 8. The waveforms that

are averaged are the voltage across Q1, v_{ap}, the voltage across CR1, v_{cp}, the current in Q1, i_a and the current in CR1, i_p. The waveforms are shown in Figure 9.

Figure 8. Buck-Boost power stage

Figure 9. Buck-Boost Waveforms

We first state some basic relationships that are used repeatedly. The terminal currents averaged over one switching cycle are given by:

$$\langle i_a \rangle = \frac{i_{pk}}{2} * d \tag{1}$$

$$\langle i_p \rangle = \frac{i_{pk}}{2} * d_2 \tag{2}$$

Since the average over one switching cycle of the voltage across the inductor is zero, the following average voltage relationships hold:

$$\langle v_{ac} \rangle = V_I$$

$$\langle v_{cp} \rangle = -V_O$$

During the time period $d\ T_s$ the current i_a starts at a value of zero and ends at the value of i_{pk}. And since the voltage across the inductor during this time is constant and equal to $V_I = \langle v_{ac} \rangle$, the following holds:

$$V_I = L\frac{\Delta i_a}{\Delta t} = L\frac{i_{pk}}{d\ T_s} \Rightarrow \langle v_{ac} \rangle = L * \frac{i_{pk}}{d\ T_s} \tag{3}$$

Similarly, during the time period $d_2\ T_s$, the current i_p starts at a value of i_{pk} and ends at zero. Also since the voltage across the inductor is equal to $-V_O = \langle v_{cp} \rangle$, the following holds:

$$V_O = L\frac{\Delta i_p}{\Delta t} = L\frac{-i_{pk}}{d\ T_s} \Rightarrow \langle v_{cp} \rangle = L * \frac{i_{pk}}{d\ T_s} \tag{4}$$

With the above four equations, we begin with the derivation of the 'input' side (v_{ac} side) of the PWM switch model.

We solve eq. (3) for i_{pk} and use $V_I = \langle v_{ac} \rangle$, then substitute into eq. (1) to get:

$$\langle i_a \rangle = V_I\frac{d^2 * T_s}{2 * L}$$

We note that the average current flowing into terminal *a* is proportional to the input voltage, V_I. We define an effective resistance as follows:

$$R_e = \frac{2 * L}{d^2 * T_s}.$$

After rearranging, we get:

$$\frac{V_I}{\langle i_a \rangle} = R_e.$$

This equation shows that the input port looks like an equivalent resistance. We can also talk about an apparent input power of $\frac{V_I^2}{R_e}$ which will be used next.

To begin the derivation of the 'output' side (v_{cp} side), we start with eq. (4), solve eq. (3) for i_{pk} and substitute back into eq. (4), we get:

$$\langle v_{cp} \rangle = \frac{\langle v_{ac} \rangle * d}{d_2}.$$

We next solve the above equation for d_2 and substitute into eq. (2) and also use i_{pk} (from eq. (3)) and substitute into eq. (2), we get after rearranging:

$$\langle i_p \rangle = \frac{\langle v_{ac} \rangle^2 d^2 T_s}{\langle v_{cp} \rangle 2L}$$

Finally, we use $\langle v_{ac} \rangle = V_I$ and substitute in the above equation to get the 'output' side relationship:

$$\langle i_p \rangle \langle v_{cp} \rangle = V_I^2 \frac{d^2 * T_s}{2 * L} = \frac{V_I^2}{R_e}.$$

This equation shows that the average output current times the average output voltage is equal to the apparent input power.

Now we can implement the above input and output relationships into an equivalent circuit model. This model is useful for determining the DC operating point of a power supply. The input port is simply modeled with a resistor, R_e. The output port is modeled as a dependent power source. This power source delivers power equal to that dissipated by the input resistor, R_e. The equivalent circuit can be constructed as follows:

Figure 10. DCM PWM Switch Model

To illustrate discontinuous conduction mode power supply analysis using this model, we examine the buck-boost converter. The analysis proceeds like the CCM case. The equivalent circuit is substituted into the original circuit. The DCM Buck-Boost converter model schematic is shown in the figure below.

Figure 11. DCM Buck-Boost Converter Model

First, the apparent power dissipated in Re is determined as:

$$P_{Re} = \frac{V_I^2}{R_e}.$$

The dependent power source delivers the above amount of power to the output load resistor, R. We can calculate the voltage gain as a function of D by equating the two powers as shown:

$$\frac{V_I^2}{R_e} = \frac{V_O^2}{R} \Rightarrow \frac{V_O}{V_I} = \sqrt{\frac{R}{R_e}} = \sqrt{\frac{R}{2*L/D^2*T_s}} = D\sqrt{\frac{R*T_s}{2*L}}.$$

Now, to derive the small signal model, the circuit of Figure 11 is perturbed following the procedure in the CCM derivation. To see the detail of the derivation, the reader is directed to reference [4] for details. The resulting small signal model for DCM is shown in the figure below.

Figure 12. Small Signal DCM PWM Switch Model

The parameters for the DCM small signal model are summarized in Table 1.

Table 1. Small Signal DCM PWM Switch Model Parameters

Where M is defined as the DC conversion ratio of the converter, i.e. $\frac{V_O}{V_I}$. A summary of DC conversion ratios for the three common converters for continuous conduction mode and for discontinuous conduction mode operation are given in Table 2.

Table 2. Summary of DC Conversion Ratios for CCM and DCM

Reference Voltage/Error Amplifier Modeling

The next control loop component shown in Figure 1 to be investigated is the reference voltage/error-amplifier combination. This circuit senses the output voltage and compares the sensed output voltage to the reference voltage. The difference between the output voltage and reference voltage is then amplified to produce an 'error signal' usually referred to as V_E. The amount of amplification or gain is designed to have a specific frequency response. The purpose of the gain and phase variation versus frequency is to add or subtract gain and phase to the remainder of the control loop such that the overall

power supply open loop response is satisfactory. In power supply literature, as well as control systems literature this design approach is known as frequency compensation.

A typical circuit configuration is shown in Figure 13.

The reference voltage is applied to the non-inverting terminal of the op-amp. When operating in tandem with the rest of the power supply, the reference voltage, V_{ref}, along with the two divider resistors, R1 and Rbias, set the power supply DC output voltage. By simple circuit analysis, the output voltage is given by:

$$V_O = V_{ref} * \left(1 + \frac{R1}{Rbias} \right).$$

To arrive at the transfer function for this circuit, we use the well-known formula for an inverting op-amp configuration:

$$G_{EA}(s) = -\frac{Z_f(s)}{Z_i(s)}$$

where $Z_f(s)$ is the impedance of the feedback components

$Z_i(s)$ is the impedance of the input components.

For example,

$$Z_f(s) = \frac{\left(R2 + \frac{1}{s * C1} \right) * \left(\frac{1}{s * C2} \right)}{\left(R2 + \frac{1}{s * C1} \right) + \left(\frac{1}{s * C2} \right)} \quad \text{and}$$

$$Z_i(s) = \frac{(R1) * \left(R3 + \frac{1}{s * C3} \right)}{(R1) + \left(R3 + \frac{1}{s * C3} \right)} .$$

Now, after simplifying, the transfer function from V_O to V_E in the frequency domain is given by:

$$G_{EA}(s) = \frac{V_E}{V_O}(s) = \frac{(-1)(1 + s * R2 * C1)(1 + s * C3 * (R1 + R3))}{(s * R1 * C1)\left(1 + s * R2 * \frac{C1 * C2}{C1 + C2} \right)(1 + s * C3 * R3)}$$

The above transfer function is used to represent the frequency response of the error-amplifier. It is used with the other two power supply transfer functions to represent the power supply control loop.

Figure 13. Typical Error-Amplifier

Note that the Error-Amplifier configuration shown in the figure provides two zeroes, two poles, and high gain at low frequencies. A zero is a factor in the *numerator* of the transfer function of the form $(1 + s * R * C)$. A pole is a similar factor to a zero but in the

denominator of the transfer function. These characteristics are normally required for frequency compensation of a voltage-mode controlled continuous conduction mode buck regulator. However, presenting design procedures for compensation of power supply control loops is beyond the scope of this work. Armed with good power supply modeling techniques and a good undergraduate text on control systems, the power supply designer can proceed successfully.

Pulse-Width-Modulator Modeling

The last control loop component shown in Figure 1 to be examined is the pulse-width-modulator. In the broadest sense, the pulse-width-modulator converts an analog input voltage to a repetitive train of logic level pulses. The pulse train is usually a fixed frequency while the width of the pulses is dependent on the analog input voltage. In switching power supplies, this logic level pulse train is generally referred to as the PWM output. The two most popular switching power supply control strategies that make use of a pulse-width-modulator are voltage-mode control and current-mode control. Voltage-mode control will be discussed first by giving a review of its general operation. After that, the frequency response of this PWM method is presented. Current-mode control will be covered in a similar fashion later. Although there are variable frequency modulation schemes in use, our discussion will be limited to fixed frequency operation.

Voltage-Mode Control

The pulse-width-modulator accepts the error-amplifier output voltage, V_E, as its input. The PWM output is a logic signal called *d(t)*. The actual circuit implementation of a voltage-mode control pulse-width-modulator is simply a ramp generator and a comparator. Figure 14 shows a simplified schematic of a pulse-width-modulator. The ramp waveform can be either a sawtooth waveform or a triangle waveform. The comparator's two inputs are the ramp waveform and the error-amplifier output voltage, V_E. This comparator is usually referred to as the PWM comparator. As the ramp waveform varies from its minimum level to its maximum, the output of the PWM comparator switches from a high level to a low level, with the transition occurring when the two comparator inputs are equal. Since the ramp waveform is a fixed frequency, so is the PWM output. Similarly, since the PWM output is a fixed frequency that drives the power stage, this frequency becomes the power supply switching frequency.

Figure 14. Typical Pulse Width Modulator

Figure 15 gives representative waveforms for a pulse-width-modulator with a triangle waveform used as the ramp. Notice in the figure that as V_E increases, the width of the output voltage pulses, *d(t)*, also increases. Another important thing to notice is the peak-to-peak amplitude of the triangle wave. This value is V_M and is used in the derivation for the gain of the pulse-width-modulator.

Now, referring to Figure 16, if V_E is below the minimum level of the triangle wave, V_{low}, the PWM output is constantly low. A low PWM output corresponds to $d(t) = 0$. If V_E goes above the maximum level of the triangle wave, V_{high}, the PWM output is constantly

high. A high PWM output corresponds to *d(t)* = 1. As shown in the figure, the width of d(t) increases linearly as VE increases from V_{low} to V_{high}. So the 'gain' from V_E to *d(t)* is defined as the change in duty cycle for a change in error voltage (in the linear region). In an equation, the relationship is:

$$G_{PWM} = \frac{\Delta\, d(t)}{\Delta\, V_E} = \frac{1-0}{V_{HIGH} - V_{LOW}} = \frac{1}{V_M}$$

where V_M = the peak-to-peak amplitude of the ramp waveform. Notice that the above transfer function has no dependence on frequency. This is a simplification and is accurate for frequencies below half of the power supply switching frequency. When modeling a power supply control loop, we are normally only interested in frequencies up to the open loop crossover frequency which is usually less than one-tenth of the switching frequency.

The above transfer function is used to represent the frequency response of the pulse-width-modulator. It is used with the other two transfer functions to represent the power supply control loop.

Figure 15. PWM Illustration

Conclusion

This paper has presented the powerful yet simple technique of using the PWM Switch to model switching power supply power stages. The PWM Switch can model power stages operating in continuous conduction mode or discontinuous conduction mode.

References

Any good undergraduate level control systems textbook.

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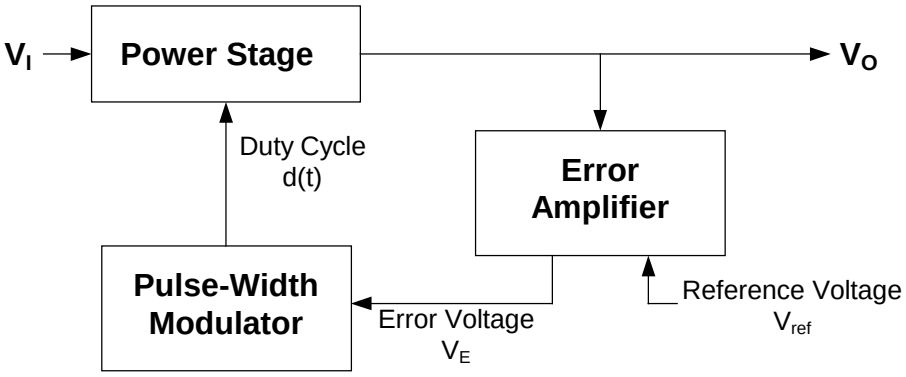

Figure 1. Power Supply Control Loop Components

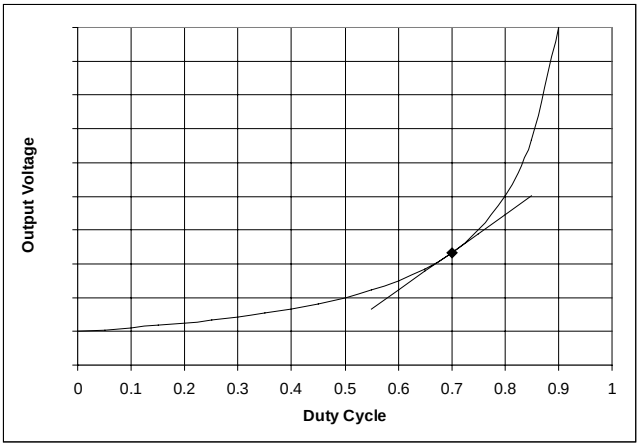

Figure 2. Boost Power Stage Gain vs. Duty Cycle

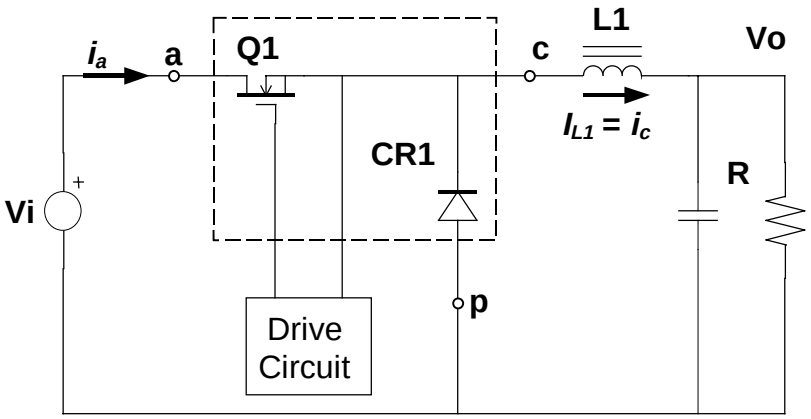

Figure 3. Buck Converter Power Stage

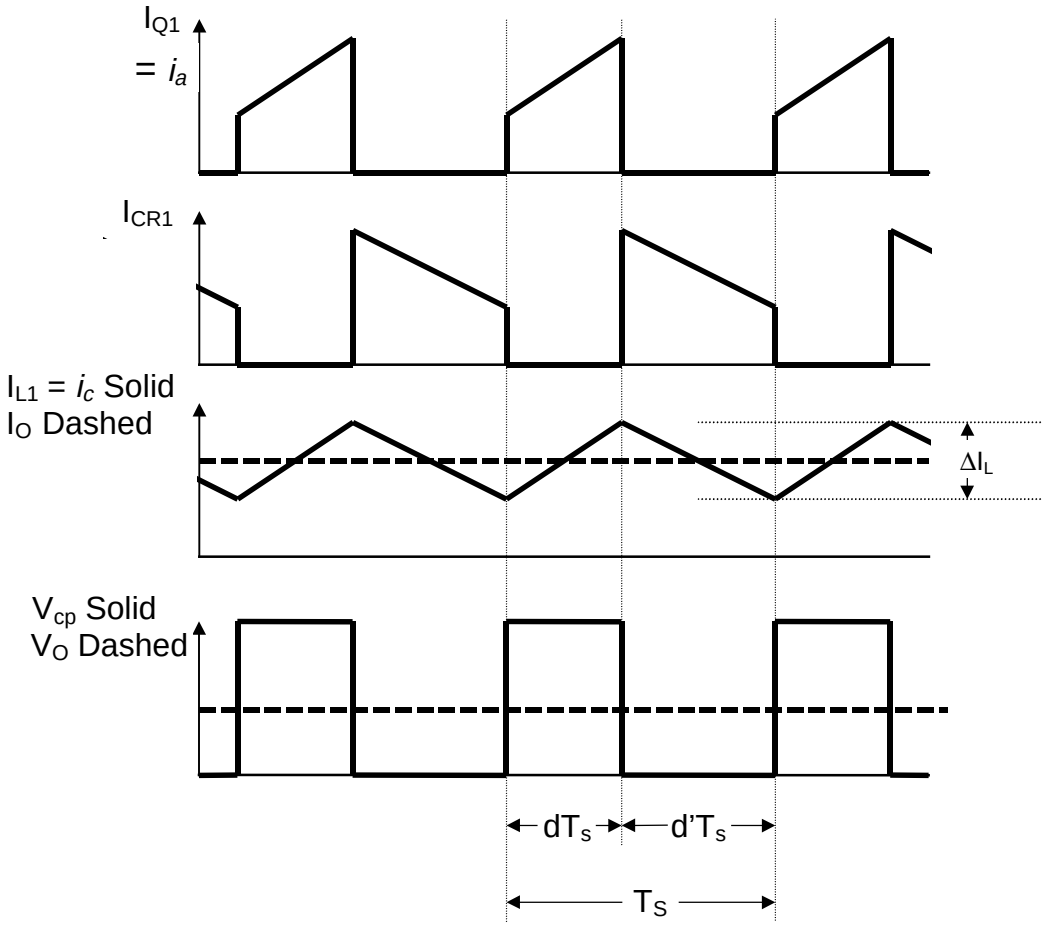

Figure 4. Buck Converter Waveforms

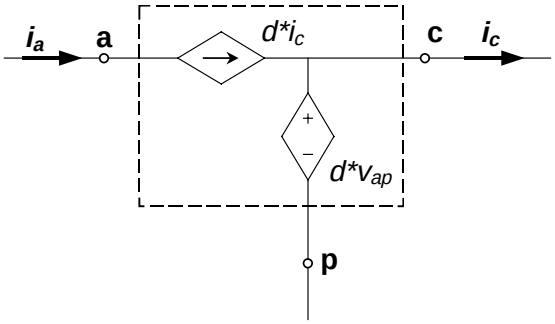

Figure 5. Averaged (nonlinear) CCM PWM Switch Model

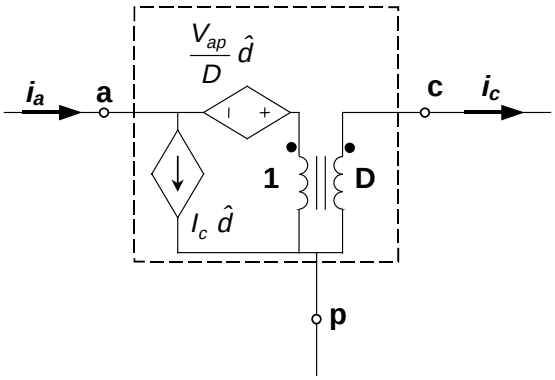

Figure 6. DC and Small Signal CCM PWM Switch Model

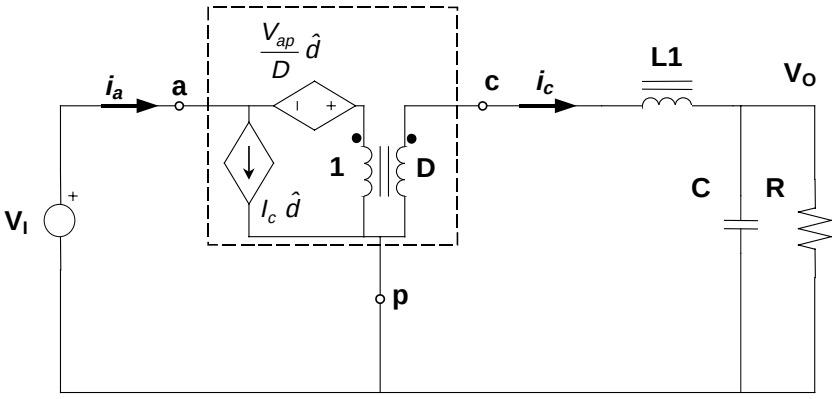

Figure 7. CCM Buck Converter Model

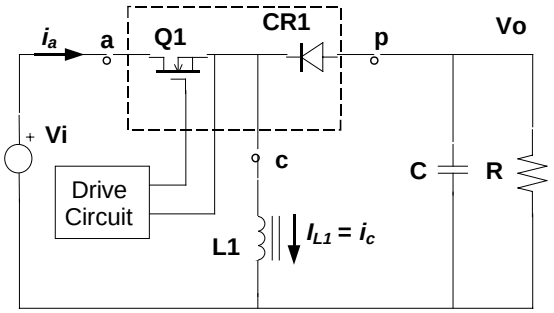

Figure 8. Buck-Boost power stage

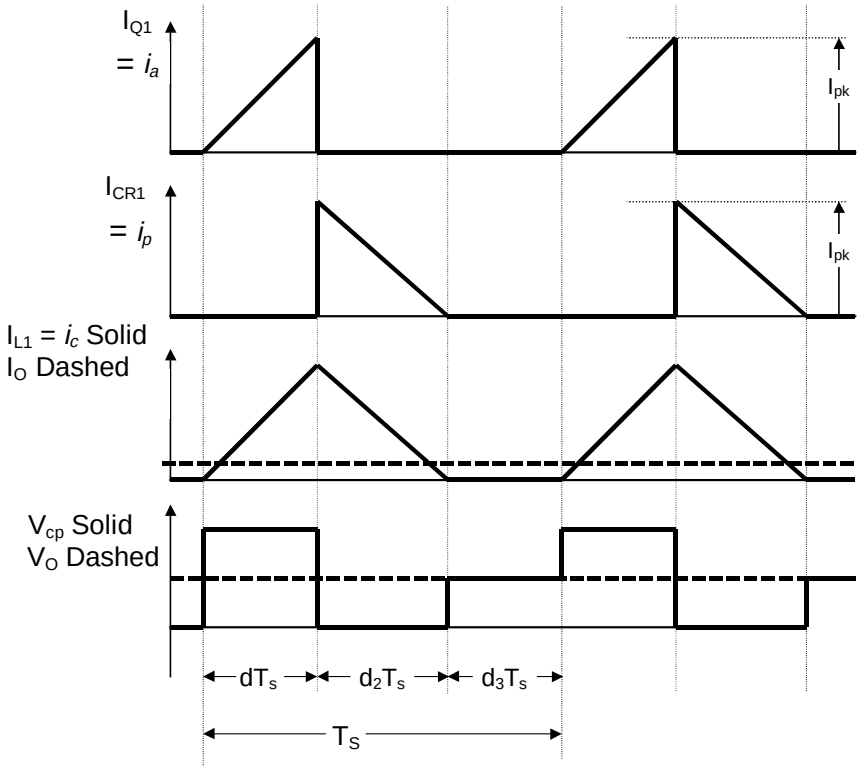

Figure 9. Buck-Boost Waveforms

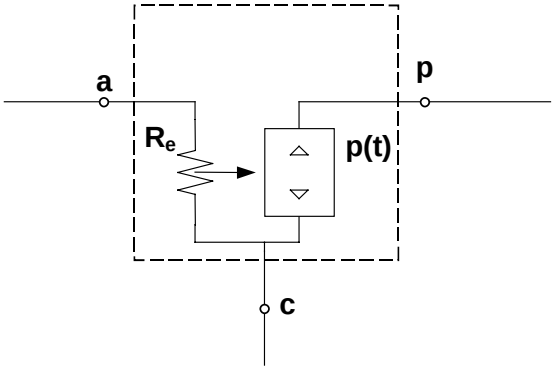

Figure 10. DCM PWM Switch Model

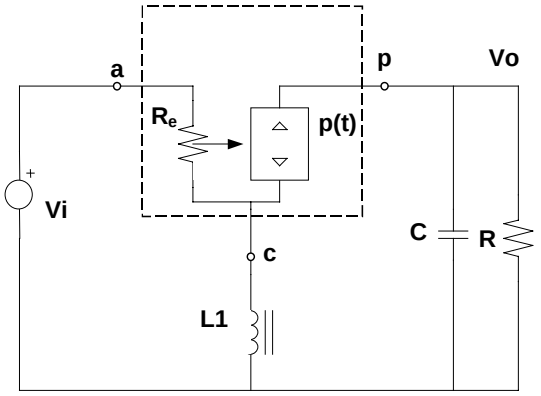

Figure 11. DCM Buck-Boost Converter Model

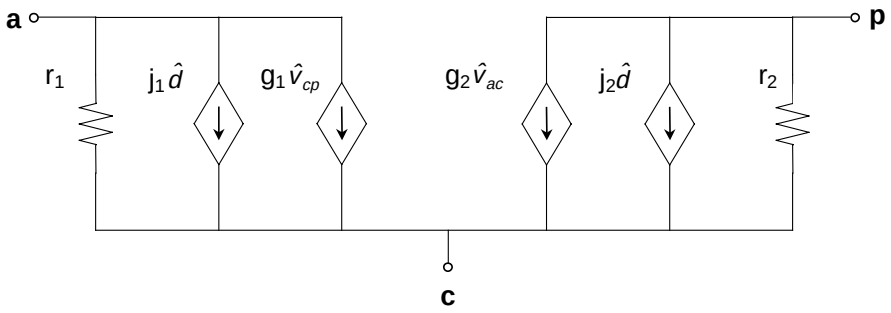

Figure 12. Small Signal DCM PWM Switch Model

Table 1. Small Signal DCM PWM Switch Model Parameters

Power Stage	g_1	j_1	r_1	g_2	j_2	r_2
Buck	$\frac{1}{R_e}$	$\frac{2(1-M)V_{ac}}{DR_e}$	R_e	$\frac{2-M}{MR_e}$	$\frac{2(1-M)V_{ac}}{DMR_e}$	M^2R_e
Boost	$\frac{1}{(M-1)^2 R_e}$	$\frac{2MV_{ac}}{D(M-1)R_e}$	$\frac{(M-1)^2}{M}R_e$	$\frac{2M-1}{(M-1)^2 R_e}$	$\frac{2V_{ac}}{D(M-1)R_e}$	$(M-1)^2 R_e$
Buck-Boost	0	$\frac{2V_{ac}}{D R_e}$	R_e	$\frac{2}{MR_e}$	$\frac{2V_{ac}}{DMR_e}$	M^2R_e

Table 2. Summary of DC Conversion Ratios for CCM and DCM

Power Stage	M (CCM)	M (DCM)
Buck	D	$\frac{2}{1+\sqrt{1+4\frac{R_e}{R}}}$
Boost	$\frac{1}{1-D}$	$\frac{1+\sqrt{1+4\frac{R}{R_e}}}{2}$
Buck-Boost	$\frac{-D}{1-D}$	$-\sqrt{\frac{R}{R_e}}$

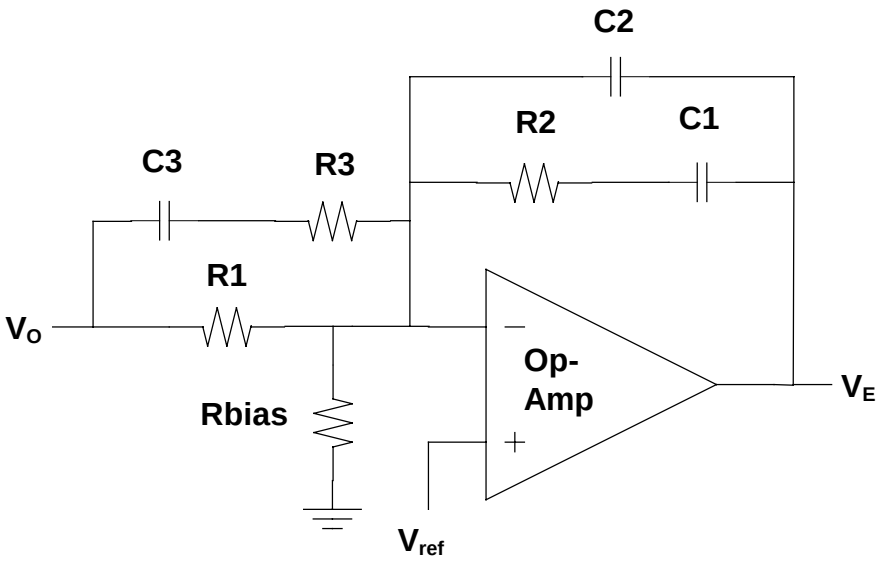

Figure 13. Typical Error-Amplifier

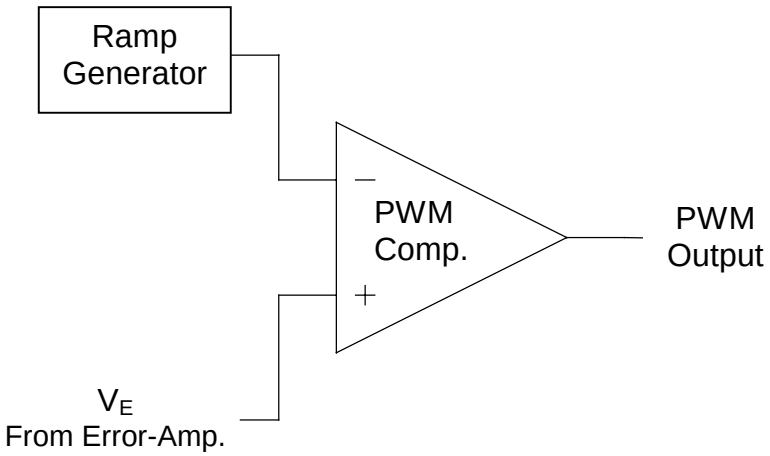

Figure 14. Typical Pulse Width Modulator

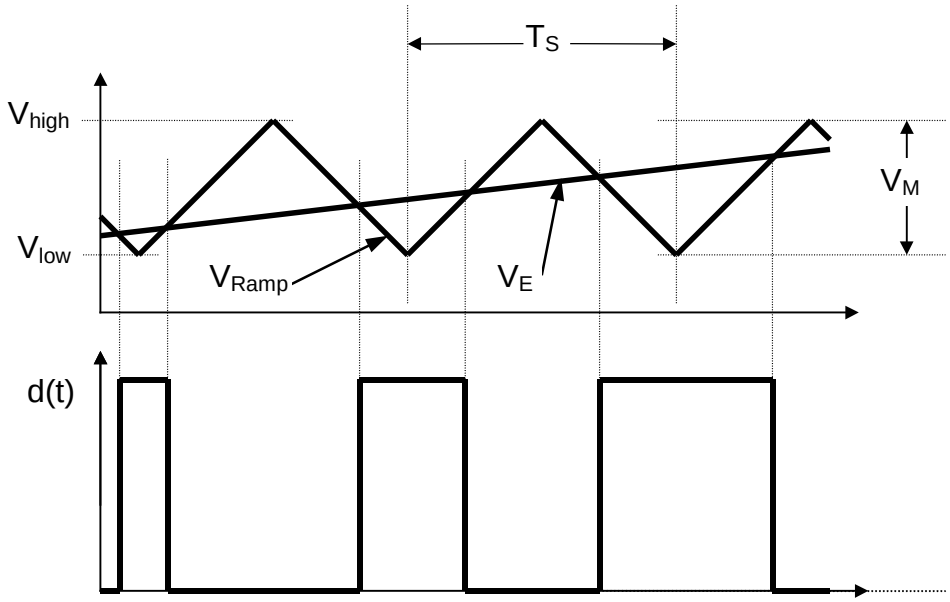

Figure 15. PWM Illustration