New High Speed Technique for Pipeline ADC design
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The pipeline architecture for A/D converters has gained wide popularity because of low power and low component count advantage over flash or semi-flash design. Many research projects are ongoing to increase its speed and resolution and reduce its power. Parallel pipeline architecture is increasingly being used to achieve higher speeds. However, offset, gain error and clock jitter usually limits the resolution to less than 8 bits, with 10 bits requiring some kind of calibration [2]. Also, the power is many times that of a single pipeline.

A typical pipeline block is shown in figure 1. It consists of a sub-ADC, sub-DAC and a subtractor. The resulting voltage is then multiplied by the stage gain which is usually 2 to the power the number of bits/stage. The complete pipeline A/D converter consists of cascading many stages together. All the stages can be identical if simplicity of design is required. To optimize power and die area, scaling is needed since the resolution requirements for each stage drop by the number of bits resolved as we go down the pipeline. The digital outputs are aligned by delaying the bits of each stage by the appropriate number of clock cycles.

One of the advantages of a pipeline architecture is its low component count which increases linearly with resolution as compared to a flash which increases exponentially. The reason for that is the concurrent processing of its analog input. Also the power dissipation is much lower than that of a flash or a semi-flash. Another advantage is its immunity to comparator offset. This is accomplished by the redundancy technique, in which more bits are resolved per stage (Usually half a bit). The resulting most significant bit is later added to the previous stage. This procedure is done for all the pipeline stages in a ripple carry manner.

The number of bits/stage resolved greatly affect the linearity and performance of the ADC. A high number of bits/stage requires a large number of comparators for the sub-ADC and places a high requirement on the bandwidth of the opamp due to the high closed loop gain needed to map the residue back to the original reference levels. The advantage is usually less sensitivity to component mismatch and a small number of stages. A low number of bits/stage will result in an easier design and higher bandwidth. The drawback is usually more sensitivity to component mismatch and worse linearity and spurious free dynamic range (SFDR) for a given component mismatch distribution. This could be a problem for resolutions higher than 10 bits.

So in order to achieve the highest possible speed, a 1 bit/stage is recommended. The pipeline block for a 1 bit/stage can be easily implemented using a simple switched capacitor opamp based circuit. A gain of 2 requires 3 unit capacitors (2 sampling capacitors, and one in the feedback loop). One way to implement this

circuit with only 2 capacitors is shown in Figure 2.

This diagram (And all following block diagrams) is a single ended representation of the circuit. The actual design is fully differential to maximize the PSRR (Power supply rejection ratio) and to minimize the second order harmonics. The overall gain is 2. This is achieved by having one of the sampling capacitors placed in the feedback during amplification mode and placing the comparator references at 1/4 the input reference. The major advantage of this circuit is its high feedback factor and bandwidth [1]. This translates into easier requirements for both the bandwidth and the open loop gain of the opamp. Please note that we are using 1.5 bit/stage instead of 1 bit/stage for redundancy and comparator offset cancellation [1]. Since we only need 1.5 bits, 2 comparators are required for the flash sub-ADC.

We are proposing a new switched capacitor gain stage which can be used as a building block in a pipeline A/D converter. This stage can achieve higher (Almost twice) the conversion rate of a single pipeline. In general, the conversion speed of such architecture is limited by the settling time of the opamp in a closed loop configuration. The design of the new stage places the opamp in an operating point beyond unity gain during amplification mode, which allows to achieve a settling time of less than 4 ns to a 10 bit accuracy. A 10 bit 60 MSPS A/D converter was designed using this stage and implemented in a 0.4 um CMOS. The anticipated power dissipation is 36 mW, the lowest reported to date for such a high speed converter. Also, an 8 bit 80 MSPS designed using the same scheme is in fabrication. It uses the same process (CMOS 0.4 um).

Figure 3 shows a block diagram of the new stage. During sampling mode the input is sampled on capacitors C1 and C2, while C3 is discharged to GND. During amplification mode, both C2 and C3 are placed in the feedback loop while C1 is switched to the reference values depending on the digital code of the 1.5 bit ADC stage. This setup places the opamp at twice the unity gain point, therefore achieving twice the bandwidth of what is being used today. This allowed the use of large sampling capacitors in order to achieve high resolution and operate at less than 3 mW/stage. Also because of the new configuration, the output swing is reduced in half, which decreased the slew rate requirement of the opamp.

If we assume the input parasitic capacitor of the opamp to be roughly a unit capacitor, the 1/feedback factor for this stage is (C2+C3+C1+Cp)/(C2+C3)=2 as compared to 3 for the stage in figure 2. This translates into a more relaxed requirement for the open loop gain of the opamp.

The opamp used is a modified telescopic opamp. The schematic of the opamp is shown in Figure 4. This opamp type was used because of its stability above unity gain and high bandwidth. The open loop gain of the opamp is 75 dB. Its unity gain bandwidth is 650 Mhz (1pF load) and a 60 degrees phase margin.

The proposed new stage can be cascaded and used for the first few stages in the pipeline. Because the output voltage range gets divided by 2 after each stage, we need to divide the reference level for the 2nd stage by 2, for the 3rd stage by 4, and so on. This division can be accomplished either by a simple resistor divider or by scaling the capacitors as shown in figure 5 and figure 6 for the second and the third stage respectively. It is important to mention that reducing the range after each stage does not affect the signal to noise ratio of the overall ADC because the accuracy requirement of the converter drops by 6 dB after each bit resolved and because the converter is not KT/C noise limited (Usually, if the resolution of the converter is less than 10 bits, the capacitor sizing is designed to meet the matching requirements, which in most processes exceeds the KT/C requirements by a large margin). The operation and bandwidth of the stages shown in Figure 5 or Figure 6 is similar to the previous stage, except that only a fraction of the sampling capacitor C1 gets switched to the reference voltages.

The drawback of this new design is that now we have to match multi capacitors instead of 2. However, with a good double poly process, matching the capacitors to 10 bit resolution is usually not a problem. Another limitation is the offset voltage of the comparators. When the reference range gets divided by 2^N, where N is the number of stages used, the resulting range should be at least twice the max offset of the comparators. At this point, we need to switch back to the conventional stage with a reduced reference voltage. The block diagram of this stage is shown in Figure 7. This stage can be used for the rest of the pipeline without any further reduction in the range. Also designing this last stage is relatively simple, because the accuracy needed is just the ADC resolution minus (N+0.5 bit).

Figure 8 shows the ideal residue plot for all the stages described above, with the only difference being the different Vr used throughout the stages.

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