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# Designing Power Supplies for TMS320VC549 DSP Systems

## Application Report

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# *Designing Power Supplies For TMS320VC549 DSP Systems*

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## Introduction

Digital Signal Processors (DSPs) are becoming more common in electronic systems. True system cost effectiveness requires that the power supply used by the DSP also be properly sized and specified. Many DSPs operate on a single 5-V or 3.3-V system supply and do not require special interfaces. The Texas Instruments TMS320VC549 is one of a new breed of dual-powered DSPs that optimize power dissipation and speed considerations by using separate core and I/O supplies. Circuitry must be provided around the DSP and converter modules to ensure that differential input voltage levels at the DSP inputs remain within safe operating levels. This report discusses several examples for powering the TMS320VC549 (VC549) Fixed-Point Digital Signal Processor.

Core power supply voltage requirements continue to decrease in order to reduce power dissipation within the device, thus allowing increased performance with faster thru-put. CMOS DSPs, such as the VC549, dissipate very little power during their static states. However, during transitions, the DSP gates look like charging capacitive loads with significant surge currents. These transient currents (in the megahertz range and above), caused by the high-speed operations within the DSP, cannot be handled by the power supply alone due to closed loop response limits within the control loop itself. Even linear regulators, which are typically much faster than switching regulators, have a loop response only in the tens of kilohertz. Since regulator response is so slow, transient current energy is provided by bypass capacitors located near the DSP at each of the supply voltage terminals. Placement of these bypass capacitors in close proximity to the DSP source terminals is critical to minimize loop inductance that creates transient spikes.

The application report, “Calculation of TMS320C54x Power Dissipation” (Texas Instruments literature number SPRA164), characterizes the worst-case input current requirements for the core at 1.1 mA per MHz of CLKOUT with a conservative overestimated value of 1.5 mA per MHz to provide for peripherals. At 100 MHZ, the total core current available should be 150 mA. Additional information concerning power requirements for various DSP configurations may be obtained from the above-mentioned report.

This report will discuss:

- ✓ Power-up/power-down sequencing of multiple sources.
- ✓ Design of linear single- and dual-source regulators.
- ✓ Layout considerations for analog circuits to reduce noise generation and pickup.

## General Considerations

During low-power modes implemented by the VC549 (IDLE1, IDLE2, and IDLE3), input current requirements are greatly reduced. Current demand drops down to a maximum of 1 μA during IDLE3. In order to take full advantage of these low-power modes, the power supply quiescent current must be reduced proportionally. Many voltage regulators can be placed into low-power modes by shutting down their outputs; not a good solution if monitoring of interrupt lines by the DSP is required. A better solution would be to power down the regulators during standby and power the VC549 with current provided by a set of resistor dividers from the main input source.

Wake-up timing is also a concern in these low-power modes. Power supplies require some finite amount of time to power up their control circuits and begin operation. Typically, power supplies reach their operating voltage in 100 μs to 100 ms. This represents an eternity to a DSP. When using a secondary supply to maintain DSP operation in low-power modes, sufficient time must be given for the primary supply to begin regulating before the DSP can be fully utilized. This may not appear to be acceptable, but is an engineering tradeoff between low-power usage when the system is not being used and speed of response during wake-up. Care should also be exercised to insure that the primary and secondary sources will operate without latchup or shutdown problems caused by the two source outputs being connected together.

At power-up and power-down, the two power supplies used for the VC549 DSP should track each other. If this cannot be guaranteed by design, then two signal diodes and a Schottky diode (D1, D2, D3) should be used between the 3.3-V source and the 2.5-V source as shown in Figure 1 on the next page. This circuit insures that the 3.3-V source will never exceed the 2.5-V source by more than 2 V and that the 2.5-V source will never exceed the 3.3-V source by more than 0.5 V. This is a requirement of the DSP to prevent damage internally due to back-biasing caused by the two voltages. This circuit will also help prevent damage to the DSP in case an external short develops on one of the power busses. In this case, the diodes should be able to handle the full short-circuit current of the power sources.

## EXAMPLE 1: 3.3-V to 2.5-V Supply

### Design Criteria

In a system with an existing 3.3-V power source capable of supplying the DSP I/O power requirements, only a core supply needs to be added. The core power supply will be a 2.5-V, +/- 5% regulator with at least 150-mA of output current, sufficient for operating the VC549 up to 100 MHz. During IDLE mode, the system current draw will be less than 10 μA.

### Specifications

Input voltage range ..... 2.97 V to 3.63 V
Output voltage range..... 2.38 V to 2.62 V
Output current range.....0 to 150 mA
Max Output ripple.....75 mV
IDLE3-mode current (total)..... 10 μA
Operating ambient temperature range..... $0^{O}$C to $125^{O}$C
Maximum I/O delta voltage during startup.....2 V

### Design

Since the system supply and the source supply requirement for the core regulator is 3.3 V, the core regulator design is straight-forward. Several regulators in the TPS7xxx families of low-dropout (LDO) regulators can be used for the 2.5-V supply, including the TPS71025 fixed 2.5-V regulator or the TPS7101and the TPS7301 adjustable output regulators. The TPS7101 is implemented in the following design only to show the steps involved in the design of an adjustable regulator. If using a fixed output voltage regulator, the steps concerning the selection of the resistor divider can be deleted.

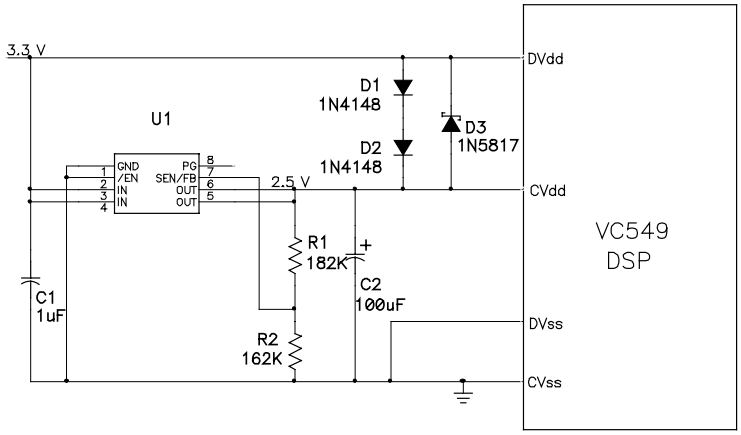


**Figure 1 Basic 2.5-V Regulator**

Resistors R1 and R2 are chosen as follows:

R2 is selected as 162 kΩ. A value close to 169 kΩ is recommended, larger values will not allow sufficient current flow in the divider for good regulation and smaller values waste power. The value of R1 is calculated to give the desired output voltage with standard 1% resistor values.

$$R1 = \frac{(V_O - 1.182)}{1.182} * R2 = \frac{(2.5 - 1.182)}{1.182} * 162\,k\Omega = 181 k\Omega \quad \Rightarrow \quad 182\,k\Omega$$

C1 is used to suppress input transients to the regulator. Depending upon the source and load conditions, typical values for C1 are 0.1 µF to 1 µF. If the 3.3-V source is far from this regulator (greater than approximately 3 inches), additional bulk capacitance may be required on the input (10-µF per 100-mA of load current is suggested as a starting point). C2 provides load transient energy for the high-speed current pulses required by the DSP and is required for stability of the LDO. A 10-µF capacitor (or larger) is recommended for the TPS7xxx series of regulators for good stability under all load conditions. A 100-uF OS-Con output capacitor with very low ESR (less than 0.1Ω at 100 kHz) is used in this design for excellent high-speed characteristics and low output ripple. Figure 1 shows the basic VC549 power supply for a 3.3-V system. A tight, well-planned layout will minimize loop inductance that can cause ringing when high current transients occur.

The basic design now has to be enhanced to meet the other requirements of the design. During the lowest-power states, the maximum input current requirement to the DSP is only 1 µA. When the TPS7101 is turned on, quiescent current is about 285 µA. In order to enter a low-power state, the TPS7101 will be shut down and replaced with a bleeder supply consisting of R3, R1, and R2 as shown in the schematic below. This will supply the 2.5-V power during IDLE with a current draw less than 10 µA. A D latch is used to control the enable signal to the LDO regulator. The latch is reset (LDO disabled) by a signal from the DSP when it enters the IDLE3 mode. The latch is set (LDO enabled) by an external signal. An external signal generated by the system will usually be required for power-on due to the 100-us delay from enable until the LDO output voltage is up and stable. The interrupt signal to the DSP could be used if sufficient time is given before actual commands are given to the DSP. The complete schematic for this configuration is shown below in figure 2.

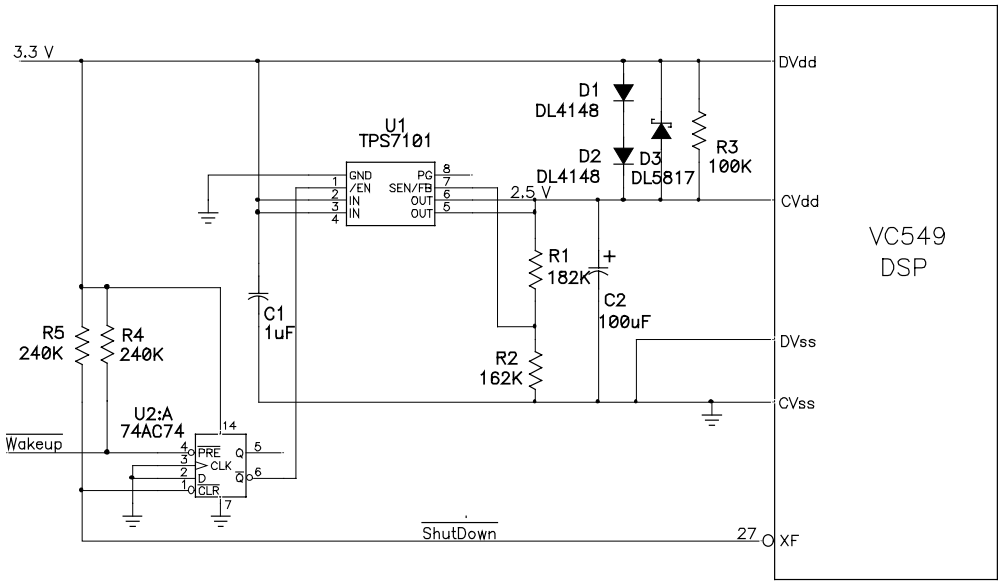


**Figure 2 Complete 3.3-V to 2.5-V DSP Regulator w/Low-Power Mode**

To calculate the value of R3 in Figure 2, the IDLE-mode current must be taken into account since it represents a significant portion of the bleeder supply quiescent current. Figure 3 shows the equivalent circuit for the low-power mode calculations. THE TMS320LC549 has a maximum IDLE3-mode current of 1 µA (with an approximate range from 0.5 to 1µA):

$$V_O = V_I - I_{Total} R_3$$

$$I_{Total} = I_{Bleeder} + I_{CPU}$$

$$V_O = I_{Bleeder} R_{1+2}$$

Combining equations and solving for R3 gives:

$$R_3 = \frac{((V_I - V_O)R_{1+2})}{(I_{CPU} R_{1+2} + V_O)}$$

Solving for R3 with the following parameters:

$V_I$ = 3.3 V
$V_O$ = 2.5 V
$R_{1+2}$ = 344 kΩ
$I_{CPU}$ = 0.75 µA

R3 = 99.8 kΩ ⇒ Use 100 kΩ

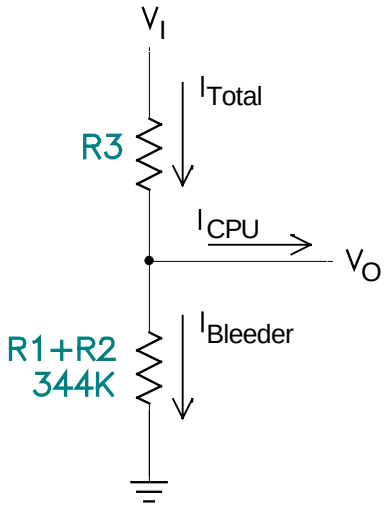


**Figure 3 Low-Power Mode Circuit**

Now substituting the new value for R3, assuming worst-case resistor tolerances of 1%, and assuming a worst-case range of IDLE3 current from 0.5 to 1 µA, the range of values for $V_O$ is calculated using this equation:

$$V_O = \frac{((V_I - R_3 I_{CPU})R_{1+2})}{(R_{1+2} + R_3)}$$

$V_O$ will range from 2.223 V to 2.774 V. This is absolute worst case with all parameters going to the extremes. Using well established statistical calculations, it can be shown that in all likelihood, the limits of this range will never be seen.

**Table 1 Bill of Material (for Figure 2)**

| Ref Des | Part Number | Description | Mfgr |
|---|---|---|---|
| C1 | ECS-T1CY105R | Capacitor, Tantalum, 1 µF, 16 V, 10% | Panasonic |
| C2 | 10SM100M | Capacitor, OS-Con, 100 µF, 10 V, 20% | Sanyo |
| D1 | DL4148 | Diode, Signal, 100 V, 10 mA | Diodes, Inc. |
| D2 | DL4148 | Diode, Signal, 100 V, 10 mA | Diodes, Inc. |
| D3 | DL5817 | Diode, Schottky, 1 A, 20 V | Diodes, Inc. |
| R1 | | Resistor, Metal Film, 182 kΩ, 1%, 1/10W | |
| R2 | | Resistor, Metal Film, 162 kΩ, 1%, 1/10W | |
| R3 | | Resistor, Metal Film, 100 kΩ, 1%, 1/10W | |
| R4 | | Resistor, Carbon Film, 240 kΩ, 5%, 1/10W | |
| R5 | | Resistor, Carbon Film, 240 kΩ, 5%, 1/10W | |
| U1 | TPS7101QD | IC, Regulator, Adjustable, 500 mA | Texas Inst. |
| U2 | SN74AC74PW | IC, Dual Positive-edge-triggered D Flip-flop | Texas Inst. |

## EXAMPLE 2: 5-V to 3.3-V and 2.5-V Supply

### Design Criteria

In this design example, a 5-V source is used to generate both the 3.3-V and 2.5-V supplies. This adds sequencing requirements to the previous design spec and an additional regulator. Power dissipation requirements will also go up due to the higher source voltage.

### Specifications

| | 3.3-V Supply | 2.5-V Supply |
|---|---|---|
| Input voltage range | 4.75 V to 5.25 V | 4.75 V to 5.25 V |
| Output voltage range | 2.97 V to 3.63 V | 2.38 V to 2.62 V |
| Output current range | 0 to 150 mA | 0 to 150 mA |
| Max output ripple | 75 mV | 75 mV |
| IDLE3-mode current (total) | 10 μA | |
| Operating ambient temperature range | -25$^{O}$C to 85$^{O}$C | -25$^{O}$C to 85$^{O}$C |
| Sequencing of output voltages | | 3.3 V then 2.5 V |

### Design

The two regulators required for this application can both be LDOs. However, there are two ways to connect these to meet the sequencing requirements. The 2.5-V regulator can be connected to the output of the 3.3-V regulator, thus insuring that the 2.5 V will come up after the 3.3 V. Connecting the regulators this way will require that all of the 2.5-V current plus the 3.3-V current will flow through the 3.3-V regulator. This will result in a maximum power dissipation for the 3.3-V regulator of:

$$P_D = \frac{\left(V_{I(Max)} - V_{O(Min)}\right)}{I_{Total}} = \frac{(5.25\,V - 2.97\,V)}{0.3\,A} = 684\,mW$$

well above the maximum power dissipation for a SO-8 package. A DIP or TSSOP PowerPad™ package could be used to get around this problem or possibly the use of a heatsink on the 3.3-V regulator.

The other alternative is to power both regulators from the 5-V source, use a NAND gate to monitor the 3.3-V output, and use this signal to control the 2.5-V regulator. This will be the approach for this design. The 3.3-V regulator will be a fixed output regulator, the TPS7233, while the 2.5-V regulator will be the same circuit used in the previous example. Low-power-mode circuitry is shown, but may be deleted if it is not a system requirement. The design is shown in figure 4 below.

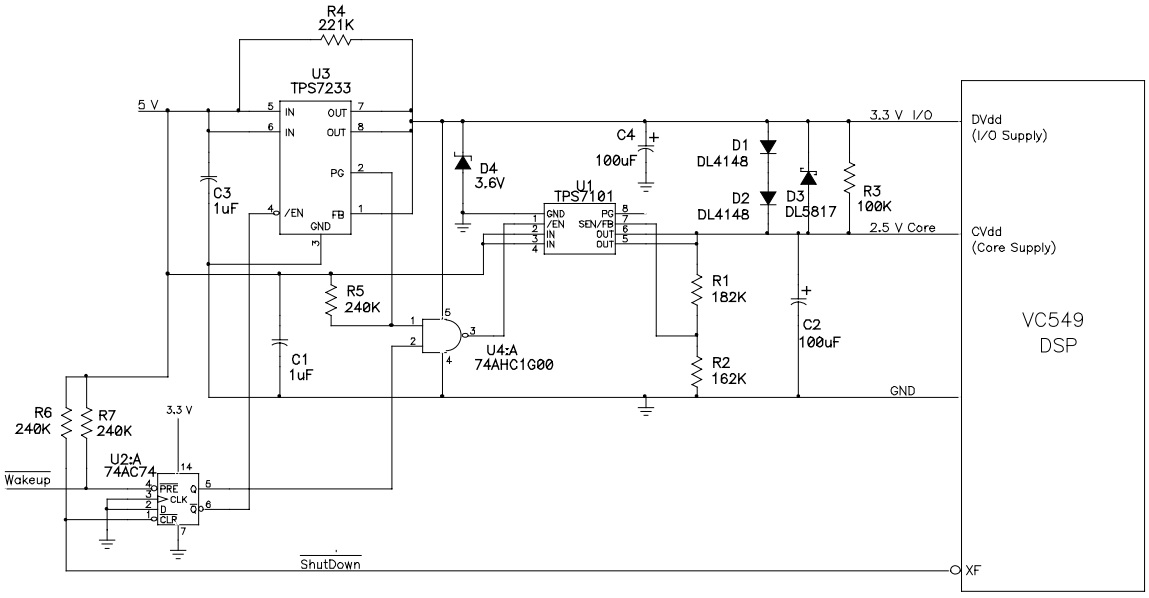


**Figure 4 5-V to 3.3-V and 2.5-V supply**

The low-power-mode circuitry functions as stated in the previous example. One addition is the Q output of U2 which is used for the sequencing circuit. The Q output of U2 is used to invert the /EN signal so that it can be used to control the 2.5-V regulator. The PG (Power Good) output of U3 is an open-collector output requiring a pull-up resistor to be used with the NAND gate. R4 (in series with R3, R1, and R2) gives a 3.3-V supply for DVdd when the DSP is in IDLE3 mode and also supplies the low-level 2.5-V divider (R3, R1, R2). Since the DSP is in IDLE3 mode, the I/O current is zero. This makes the calculation of R4 straightforward. D4 is used as an overvoltage clamp and would not normally have an operating function in the circuit. The equation for finding R4 is:

$$R_4 = \frac{(DV_{DD} - V_I)}{I_{Total}}$$

Using $DV_{DD}$ = 3.3 V, $V_I$ = 5 V, and $I_{Total}$ = 7.77 µA (Bleeder current + 0.75 µA CPU current), gives a value for R4 of 219 kΩ, use 221 kΩ.

Then, to verify the output voltage ranges of the bleeder divider use the following equations:

$$DV_{DD} = V_I - I_{Total} R_4$$

$$V_O = \frac{((V_I - R_3 I_{CPU})R_{1+2})}{(R_{1+2} + R_3)}$$

Using 1% resistors, $V_I$ = 4.75 V to 5.25 V, and $I_{CPU}$ = 0.5 to 1 µA gives a range of 2.960 V to 3.605 V for $DV_{DD}$ and
a range of 2.205 V to 2.767 V for $V_O$. Again, these are absolute worst-case limits. Note that in the equation for $V_O$, the values for $DV_{DD}$ should be substituted.

**Table 2 Dual Regulator Bill of Material ( for Figure 4)**

| Ref Des | Part Number | Description | Mfgr |
|---|---|---|---|
| C1 | ECS-T1CY105R | Capacitor, Tantalum, 1 µF, 16 V, 10% | Panasonic |
| C2 | 10SM100M | Capacitor, OS-Con, 100 µF, 10 V, 20% | Sanyo |
| C3 | ECS-T1CY105R | Capacitor, Tantalum, 1 µF, 16 V, 10% | Panasonic |
| C4 | 10SM100M | Capacitor, OS-Con, 100 µF, 10 V, 20% | Sanyo |
| D1 | DL4148 | Diode, Signal, 100 V, 10 mA | Diodes, Inc. |
| D2 | DL4148 | Diode, Signal, 100 V, 10 mA | Diodes, Inc. |
| D3 | DL5817 | Diode, Schottky, 1 A, 20 V | Diodes, Inc. |
| D4 | | Diode, Zener, 3.6 V, 5% | |
| R1 | | Resistor, Metal Film, 182 kΩ, 1%, 1/10W | |
| R2 | | Resistor, Metal Film, 162 kΩ, 1%, 1/10W | |
| R3 | | Resistor, Metal Film, 100 kΩ, 1%, 1/10W | |
| R4 | | Resistor, Metal Film, 221 kΩ, 1%, 1/10W | |
| R5 | | Resistor, Carbon Film, 240 kΩ, 5%, 1/10W | |
| R6 | | Resistor, Carbon Film, 240 kΩ, 5%, 1/10W | |
| R7 | | Resistor, Carbon Film, 240 kΩ, 5%, 1/10W | |
| U1 | TPS7101QD | IC, Regulator, Adjustable, 500 mA | Texas Inst. |
| U2 | SN74AC74PW | IC, Dual Positive-edge-triggered D Flip-flop | Texas Inst. |
| U3 | TPS7233QD | IC, Regulator, 3.3 V, 250 mA | Texas Inst. |
| U4 | SN74AHC1G00DBV | IC, Single 2-Input Positive NAND Gate | Texas Inst. |

The figures below show plots of the waveforms produced by the power-sequencing circuits shown in this example.

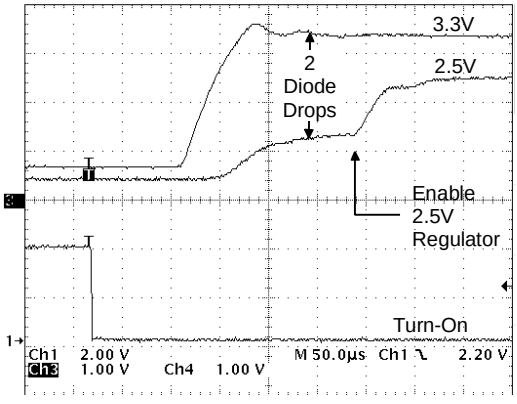


**Figure 5 DSP Power-Up**

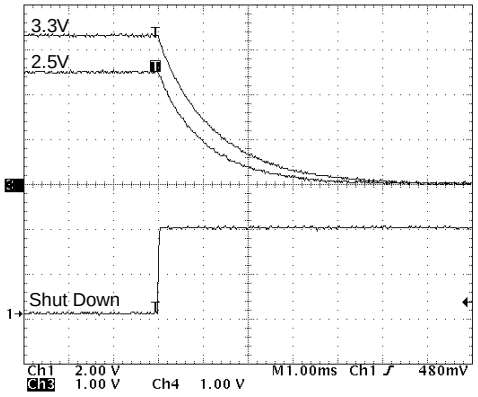


**Figure 6 DSP Power-Down**

Figure 5 shows the application of power, followed approximately 50 µs later by the increasing $DV_{DD}$

Supply. Note that the $CV_{DD}$ supply tracks $DV_{DD}$ about 2-diode drops lower, as expected, until the enable signal for the $CV_{DD}$ supply allows it to activate. At power-down (shown in figure 6), both supplies shut down immediately. Fall time is a function of the load current at the time of shutdown.

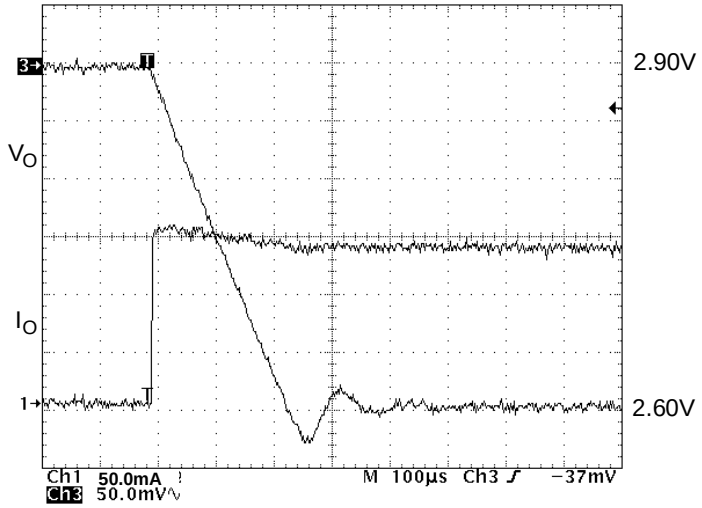


**Figure 7 Transient Waveform with 100-µF Output Capacitor**

Figure 7 shows the effect on the output voltage when the load current is stepped from a very low load (approx. 5 µA) to a high load (150 mA). The divider voltage is set to 2.90 V purposely to insure that the regulator is completely turned off during the low-current state. When the current is stepped, the output voltage drops as the output capacitor is discharged until the regulator turns on (2.60 V in this case) and begins supplying the output current. The bleed-off rate is set by the output load current and the output capacitor.

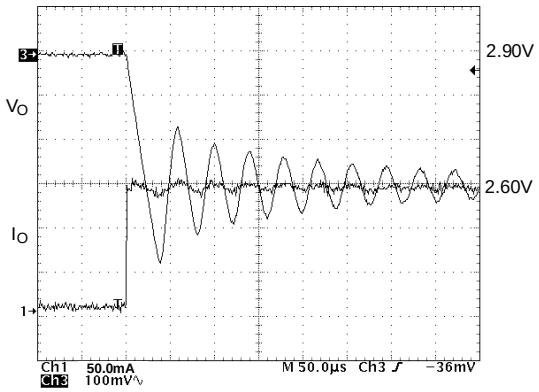


**Figure 8 Transient with 10-µF Output Capacitor**

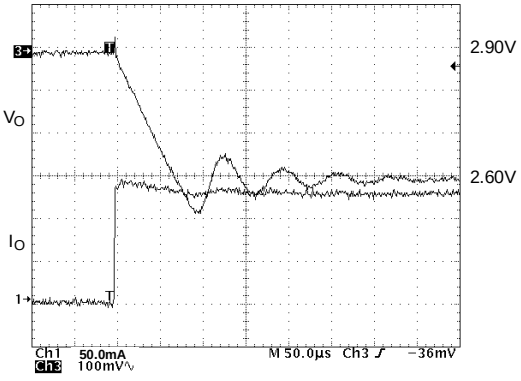


**Figure 9 Transient with 33-µF Output Capacitor**

Figures 8 and 9 show the output transient waveform when stepping the load from 5 µA to 150 mA using smaller output capacitors. Note the change in response time and undershoot with different capacitor values (Time and voltage scales are different from Figure 7). Using a smaller capacitor, such as the 10 µF used in figure 8, also produces some ringing during stepped load transients.

## Layout Information

Proper electrical design is only half of the effort required in good power supply development. Without a good layout, noise can be picked up or generated that will have a negative affect on the regulator and/or load. High-speed current transients must be properly bypassed. The regulator should be located as close as possible to the DSP. With the TMS320LC549, as is the case with most large-pin-count devices, this is not easy due to the distributed input terminals for the 2.5-V and 3.3-V inputs. Small bypass capacitors (~0.1 μF) should be placed at each input terminal and the regulator circuit should be placed near terminal 1 to be as close as possible to four of the seven input terminals. Ground planes and power planes should be used to minimize inductive pickup and to lower the source impedance of the power sources. Power supply traces should be larger than signal traces for low impedance even if they need to be trimmed down when going between IC terminals. Wider and shorter traces mean less inductance which translates to less noise generation. The input capacitor for each regulator should be very close to the input terminals and ground of the regulator. The ground plane(s) for the DSP power supplies should be physically isolated from the system ground plane(s), but connected to a single-point connection to system ground at the regulator ground pins. This will ensure that no system-ground current will flow in the DSP ground plane. An example layout of the power circuitry is shown below. The 2.5-V and 3.3-V power planes are within the DSP power ground plane area on adjacent layers.

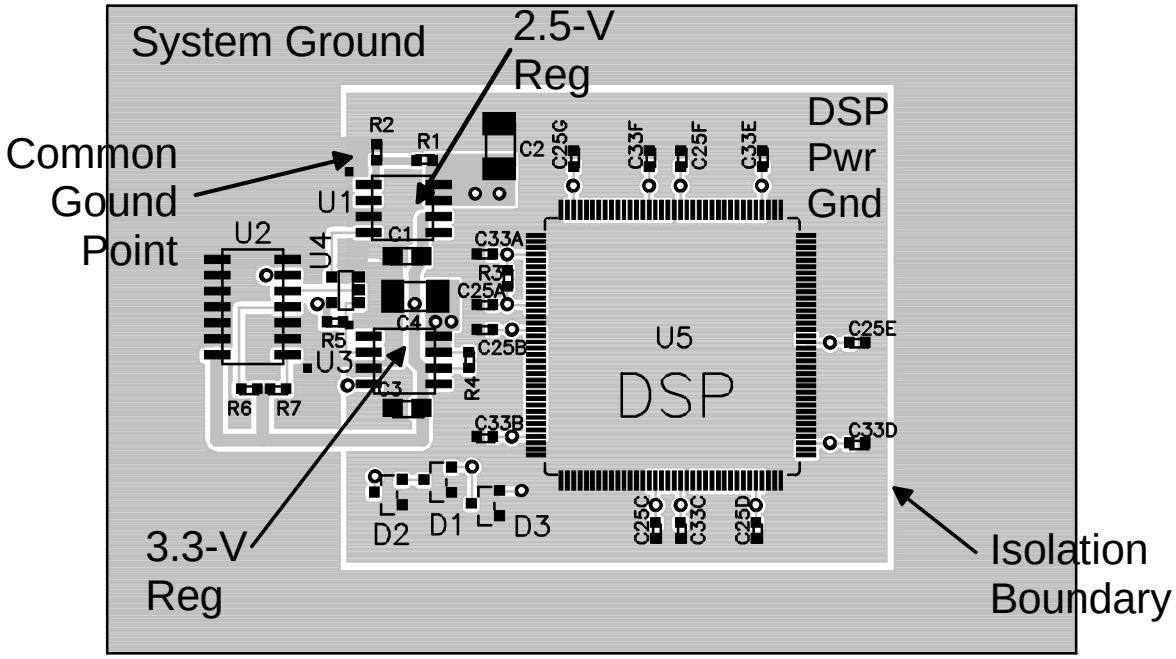


**Figure 10 Example Power Circuitry Layout**

Figure 10 shows an ideal top-plane layout for the power circuitry of a DSP using all of the points mentioned above. In reality, compromises will be made to this ideal layout due to the system requirements of the DSP circuitry. Although this will always be the case, the above considerations should be included during layout to minimize low-frequency (less than 1 MHz), power-circuit noise problems. High-frequency (greater than 100 MHz), signal noise problems relating to return paths must also be considered to pass emissions standards. Generally, the best layout

for any noise-related problems on PCBs is minimum area between a signal and its return path (and *every* signal will have a return path!).