Texas Instruments

MAY 1998
VOLUME 27

# ANALOG & MIXED-SIGNAL Showcase

## Inside



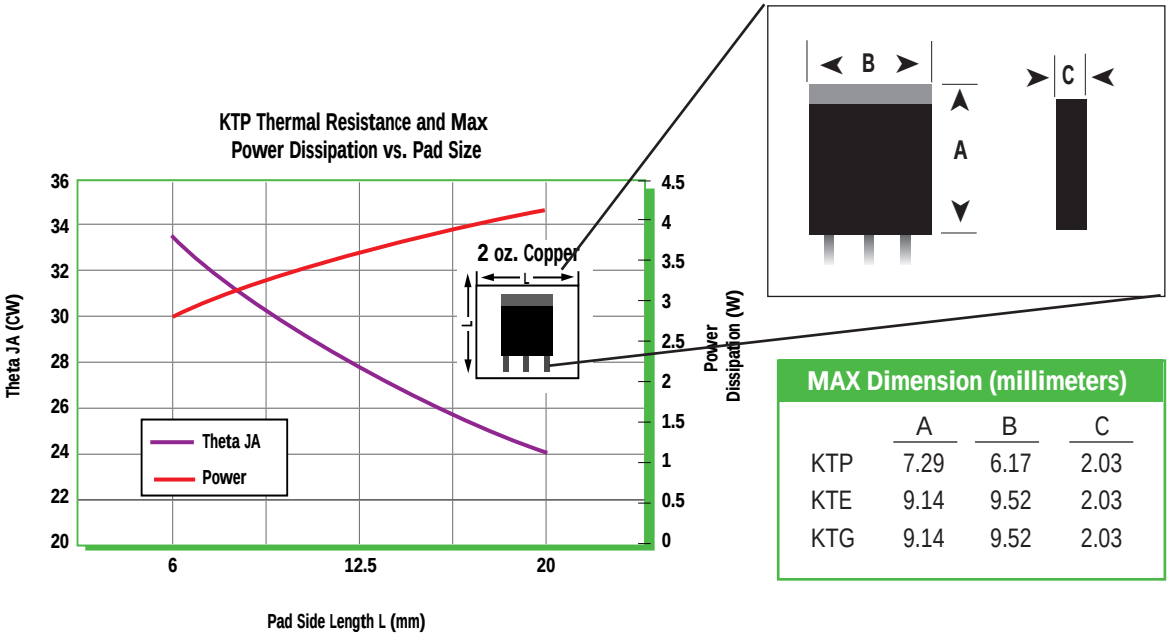

**Let TI's LVD-SCSI take you where you want to go** Page 7

## Product Features

- Low cost SMT
- Integrated heat slug
- Approximately 1.9-W power dissipation
- Low cost alternative to TO-220
- Lower profile than DPAK

# PowerFLEX™ packaging offers a low cost surface-mount alternative to TO-220

Texas Instruments now offers industry-standard voltage regulators in thermally enhanced PowerFLEX surface-mount packaging. The new PowerFLEX packages deliver excellent power dissipation capability (1.9 W for the KTE and KTG packages and 1.8 W for the KTP package) for those looking to migrate from the bulky through-hole TO-220 package. Heat sinking is accomplished by soldering the devices to a copper pad, eliminating the effort and expense of bolting a TO-220 device to the PCB in high volume manufacturing processes. The KTP package represents a significant cost saving over the standard TO-220 package available from TI, while offering the additional benefit of surface mount technology. In addition, the PowerFLEX devices are slightly smaller and lower profile than DPAK and D2PAK regulators, while remaining footprint compatible.




**MAX Dimension (millimeters)**

| | A | B | C |
|---|---|---|---|
| KTP | 7.29 | 6.17 | 2.03 |
| KTE | 9.14 | 9.52 | 2.03 |
| KTG | 9.14 | 9.52 | 2.03 |

| Device | Pin | Package |
|---|---|---|
| µA78xx | 3 | KTE |
| TL780-xx | 3 | KTE |
| TL751Mxx | 5 | KTG |
| µA78Mxx | 3 | KTP |
| µA79Mxx | 3 | KTP |
| TL750Mxx | 3 | KTP |

■ **Check box 01** for thermal data, package outlines and assembly information.

**For technical support, call (972) 644-5580.**
**To order documentation, call 1-800-477-8924, ext. 3234**

CLOCK DISTRIBUTION CIRCUITS

# Portfolio of high performance PLL clock drivers

Texas Instruments' new family of high performance phase-lock-loop (PLL) clock drivers features the CDC509, CDC516, CDC2509, CDC2510, and CDC2516. Each device is designed to precisely align, both in frequency and in phase, the feedback output (FBOUT) to the clock (CLK) input signal making the devices suitable for high end synchronous DRAM applications.

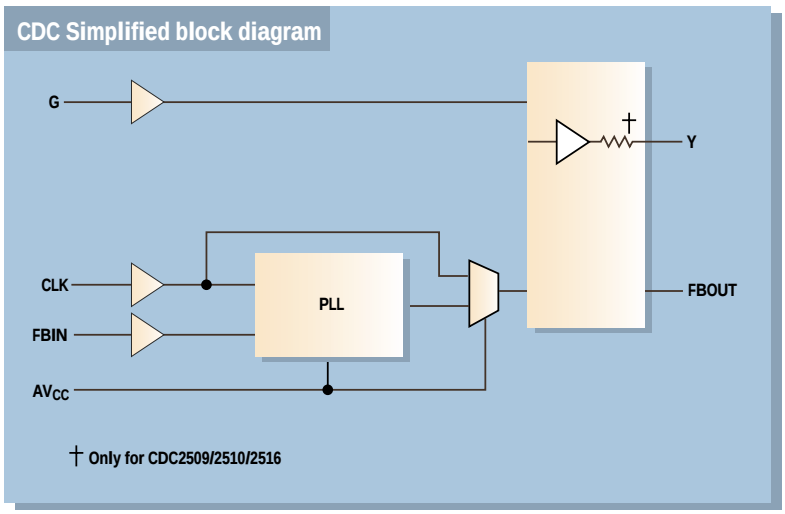
Each bank of outputs provides low-skew, low-jitter copies of the input clock. The output signal duty cycle is adjusted to 50%, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the control (G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK. When the G inputs are low, the outputs are disabled to the logic-low state.

Compared to other PLL devices, the family features integrated loop filter alleviating the need for external components reducing board space and cost. External feedback input (FBIN) enable each device to be used as a zero delay buffer. With their low voltage (3.3 V) and low power capabilities, these devices are optimized to reduce switching noise. Integrated series damping resistors make the 2000-series suitable for driving point-to-point loads. The 500-series are designed to drive multiple memory loads.

With its low cost, high performance, and zero delays, the family is designed to target high speed applications such as: SDRAM DIMMs (dual-inline memory modules) for PCs, servers, and workstations, and general purpose clocking.

The family of PLL clock drivers is available in plastic thin shrink small outline surface-mount packaging (TSSOP) for reduced printed board space requirement.

CDC Simplified block diagram




| Device | Application | Banks/Outputs | Pins/Package |
|---|---|---|---|
| CDC509 | 128M SDRAM DIMM | 1/5 & 1/4 | 24/TSSOP |
| CDC516 | 256M SDRAM DIMM | 4/4 | 48/TSSOP |
| CDC2509 | 128M SDRAM DIMM | 1/5 & 1/4 | 24/TSSOP |
| CDC2510 | 256M SDRAM DIMM | 1/10 | 24/TSSOP |
| CDC2516 | 256M SDRAM DIMM | 4/4 | 48/TSSOP |

■ **Check box 02** for a datasheet.

## Product Features

- Zero delay PLL buffers
- Low 3.3-V supply
- High operating frequency up to 125 MHz
- Integrated loop filter
- Output enable for each output bank
- Characterized for operation from 0°C to 70°C

## Suggested resale price

**Quoted per device in quantities of 10,000**

**CDC509PWR:** $4.20
**CDC516DGGR:** $4.16
**CDC2509PWR:** $4.51
**CDC2510PWR:** $4.40
**CDC2516DGGR:** $4.97

P O W E R +

# Digital control loop for

## Product Features

- RPM control with embedded DSP filter algorithm
- EEPROM registers
- Standalone operation
- Integrated driver configured for 3-Ø brushless motors
- System development software package
- Characterized for operation:
  - TPIC43T01: 0°C to 70°C
  - TPIC1310: –40°C to 125°C

## Suggested resale price

**Quoted per device in quantities of 1,000**

**TPIC43T01DA:** $2.08

**TPIC1310KTR/KTS:** $1.98

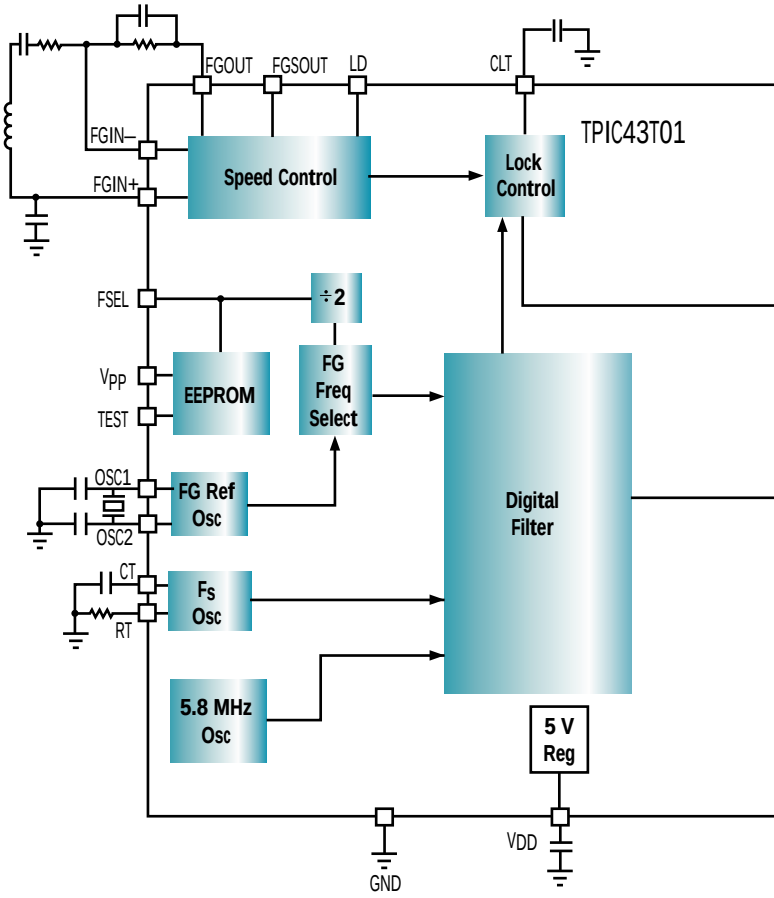
The TPIC43T01 is a monolithic device designed to provide RPM control to a 3-phase brushless DC motor. The controller is the industry's first to feature an EEPROM programmable digital filter providing increased flexibility and minimized design efforts. The TPIC43T01's gate drive outputs are designed to drive six external discrete N-channel power FETs or an integrated driver such as the new Power+ Array™ TPIC1310. As a chipset, the TPIC43T01 and TPIC1310 offer enhanced functionality and lower cost which makes it a very attractive solution for high performance motor control applications.

In addition, Texas Instruments provides a PC based Windows® compatible software package to input the motor and system characteristics and select the digital filter coefficients to stabilize the system. The software program outputs control parameters to a JEDEC compatible file to program the TPIC43T01 through a third party device programmer.

The TPIC43T01 provides a variable reluctance speed sensor interface and a Hall- effect position interface. The speed interface receives an external sinusoidal signal and converts it to a digital speed input for lock detect. The core of the control circuit is a hardware implementation of a digital signal processing algorithm consisting of a digital integrator and filter. User programmable filter coefficients set compensation pole and zero to stabilize the system response. Programmable parameters are stored in an internal EEPROM.

***TPIC43T01 Features/Benefits***

• Digital Control:
– Enables one main feedback loop to simplify design of phase-lock-loop response
– Eliminates external control loop compensation components to reduce parts count
– PWM power conversion for high efficiency
• User programmable:
– Frequency divide by select to set motor target RPM
– External speed control input for real-time select of fast/slow RPM

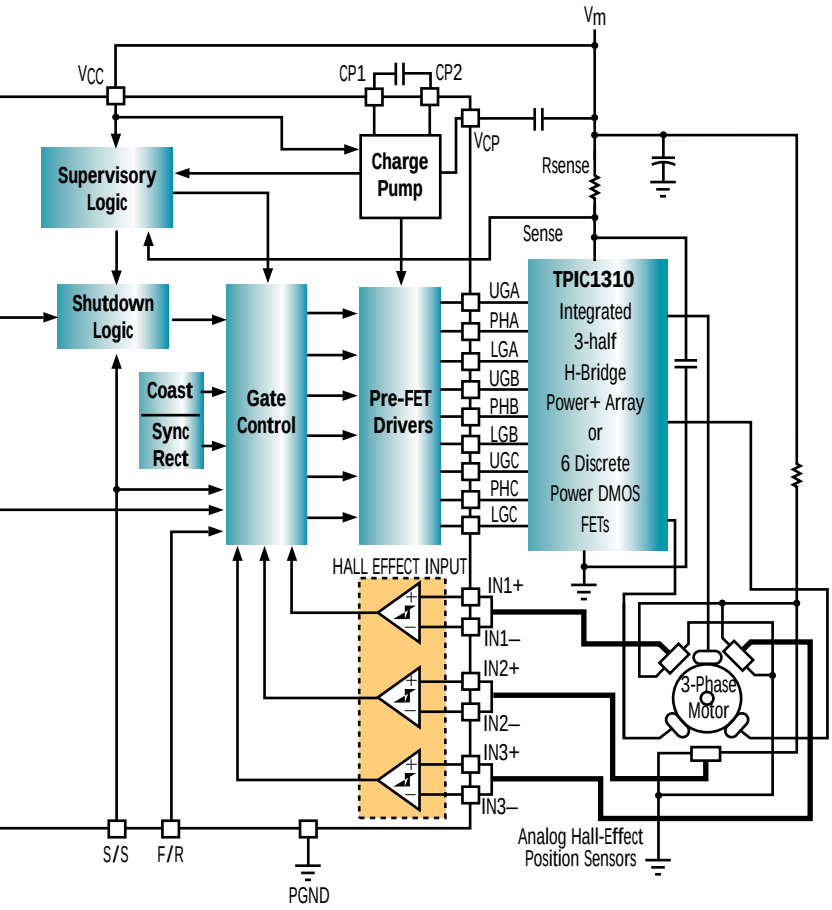


P O W E R +

# 3-phase brushless dc motor

– Improved precision allowing lower-tolerance external discrete components to reduce cost
– Digital filter pole and zero for optimized system response
– Coast mode to provide softer operation during out-of-lock conditions
– Synchronous rectification mode to recirculate current through the FETs for reducd power dissipation

• On-board functions and protection for enhanced performance and improved reliability:
– Under-voltage lockout protection
– Power-up clear
– Shutdown logic
– Watch-dog timer
– Current-limit/over-current shutdown
– Charge pump




The TPIC1310 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as a three-half H-bridge. When used with the controller TPIC43T01, the TPIC1310 allows the customer the ability to optimize the current switching capability of the output stage.

***TPIC1310 Features/Benefits***

• Low rDS(on) of 0.25 Ω for minimized power dissipation
• 30-V capability for extended voltage operation
• 3-A continuous current for increased motor drive
• Input transient and ESD protection for increased reliability

The TPIC43T01 is available in a 38-pin plastic thin small-outline surface-mount package (DA) for reduced printed board space requirement. The TPIC1310 is available in the low-cost 15-pin through-hole (KTS) and surface-mount (KTR) PowerFLEX™ packaging.

***Applications:***

• EDP – printers, copiers, fax machines, scanners, plotters
• Industrial – fans, motion control applications

■ **Check box 03** for a datasheet.

DATA TRANSMISSION

# Cost-effective gigabit ethernet transceiver

## Product Features

- Serial data rate up to 1.25 Gbps
- Compliance to IEEE 802.3 Z standard
- Low 3.3-V supply for reduced EMI
- Low power consumption of 700 mW
- High ESD protection of 6 kV
- Characterized for operation from 0°C to 70°C

The TNETE2201 gigabit ethernet transceiver is the derivative of Texas Instruments' proven Fibrechannel technology enhanced to run at 1.25 Gbps. The device is designed for ultra high speed bi-directional point-to-point data transmission over controlled impedance media of approximately 50 to 70 Ohms.

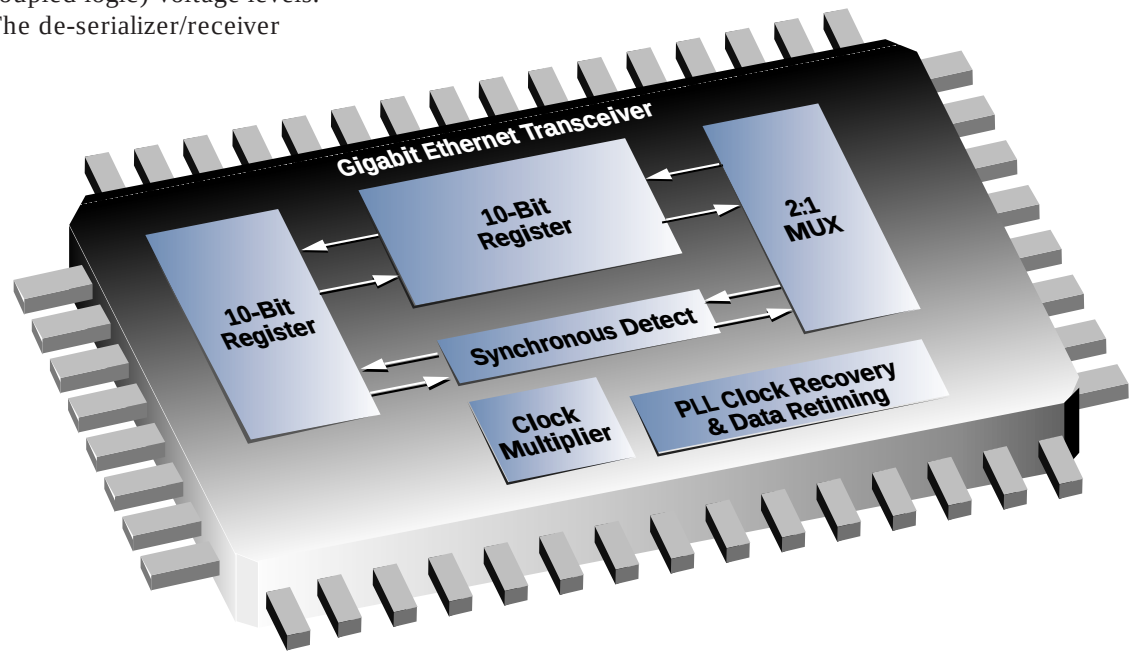
The device performs the data serialization and de-serialization function for the gigabit ethernet physical layer interface. The serializer/transmitter accepts 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially nonreturn-to-zero at pseudo-ECL (emitter coupled logic) voltage levels. The de-serializer/receiver extracts clock information from the input serial stream and de-serializes the data, outputting a parallel 10-bit data byte with respect to two receive byte clocks. The TNETE2201 also features an internal loopback capability for self-test purposes.

With its low cost, high data rate (1.25 Gbps), and compatibility, the TNETE2201 is designed to address the requirement for the next generation differential line interface circuits in the high speed networking sector such as switch-to-switch links, switch-to-server links, and backbone applications.

The TNETE2201 is available in a 64-pin thermally enhanced thin quad flat pack PJD (10mm x 10mm) or PHD (14mm x 14mm).

**End user applications:**

- Switches
- Uplink/downlink modules
- NICs (network interface cards)
- Gigabit ethernet router interfaces
- Buffered distributors




## Suggested resale price

**Quoted per device in quantities of 1,000**

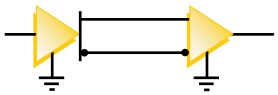
**TNETE2201PHD/PJD:** $22.25

■ **Check box 04** for a datasheet.

**For technical support, call (972) 644-5580.**
**To order documentation, call 1-800-477-8924, ext. 3234**

DATA TRANSMISSION

# Industry's first discrete dual-mode LVDS SCSI transceiver

| Standards | Circuit | Maximum Signaling Rates and Distance |
|---|---|---|
| Single-ended SCSI |  | 6 m at 10 Mxfers/s or 1.5 m at 20 Mxfers/s |
| LVD – SCSI |  | 12 m at 40 Mxfers/s |
| HVD – SCSI |  | 25 m at 20 Mxfers/s or 12 m at 40 Mxfers/s |

TI announces the SN75LVDM976, the industry's first nine-channel discrete dual-mode transceiver which supports both single-ended signaling SCSI and low-voltage differential (LVD) SCSI. The dual-mode characteristic of the SN75LVDM976 allows the flexibility of implementing LVD-SCSI in prevailing products or keeping backward compatibility with single-ended devices. Each of the nine transceivers offers electrical compatibility to both the single-ended signaling of X3.3.2-SCSI-3 Parallel Interface (Fast-20) and the new low-voltage differential signaling method of X3.227-SCSI Parallel Interface-2 (SPI-2)

The 'LVDM976 achieves dual-mode by using a window comparator incorporated by the CDE0 input to detect the status of the SCSI bus DIFFSENS line. The DIFFSENS line will be below 0.5 V if using single-ended signals, between 1.9 V and 2.4 V if using LVD, and above 2.4 V if using high-voltage differential (HVD). If HVD is detected, the output will be placed in high-impedance. Otherwise, the output will assume the characteristics of single-ended or LVD-SCSI.

The signal symmetry requirements of the Fast-40 SCSI bus means you can no longer obtain logical inversion of the signal by simply reversing the differential signal connections. The 'LVDM976 includes the INV/NON pin which gives the designer the ability to invert the logic convention. This input would be low for SCSI controllers with active-high data, and high for SCSI controllers with active-low data.

The SN75LVDM976 is ideal for applications such as disk drives and host adapter add-in boards which interface a computer system to a differential SCSI I/O subsystem. It is offered in a thin shrink small-outline package (TSSOP) with 20 mil terminal pitch, and is pin-compatible with the SN75976ADGG high-voltage differential transceiver.

■ **Check box 05** for a datasheet.

## Product Features

- Supports single-ended and LVD-SCSI
- DIFFSENS comparators on CDE0
- Pin-selectable inverting or non-inverting data path
- Receiver includes noise pulse rejection
- Power-up/down glitch protection
- Characterized for operation from 0°C to 70°C

## Suggested resale price

**Quoted per device in quantities of 1,000**

**SN75LVDM976DGG:** $8.68

**SN75LVDM976DGGR:** $8.96

W I R E L E S S

# 1.2 GHz fractional-N/integer-N synthesizer

## Product Features

- Dual (RF-IF) fractional-N PLL for 1 GHz applications
- Low voltage (2.7-5.1 V) and current (7 mA at 3.6 V) operation
- Dual modulus (32/33) RF and (4/1) IF prescalers and programmable fractional modulus (0-16)
- Normal, speed-up, and fractional compensation charge-pumps
- Characterized for operation from –40°C to 85°C

## Suggested resale price

**Quoted per device in minimum quantities of 10,000**

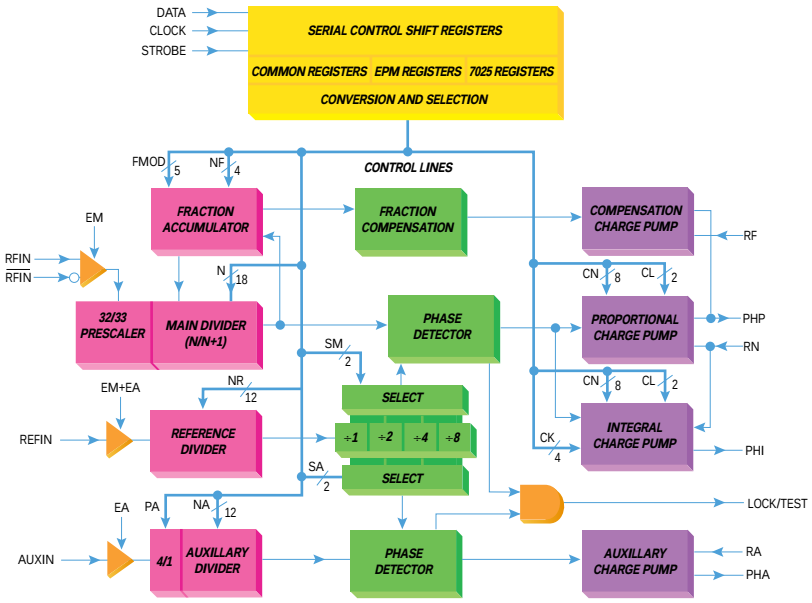
**TRF2050PW:** $3.15

The TRF2050 is a low-voltage, low-power consumption 1.2 GHz fractional-N/integer-N frequency synthesizer component for wireless applications. Along with external loops, the TRF2050 provides all functions necessary for voltage-control oscillator (VCO) control in dual phase-locked loop (PLL) frequency synthesizer systems. The main channel operates up to 1.2 GHz in support of cellular radio frequency (RF) channels. An auxiliary channel, which operates up to 125 MHz, supports most intermediate frequency (IF) channels within the RF transceiver. The operating current is typically 7.5 mA. The TRF2050 internal registers are programmed using a three-wire (Clock, Data, and Strobe) serial interface.

The current-output charge pumps directly drive passive resistance-capacitance (RC) filter networks to generate VCO control voltages. When operated in the integer-N mode, rapid main-channel frequency switching is achieved with a charge pump arrangement which enables an increased current drive and also alters the loop-filter bandwidth during the "speed-up" mode of the frequency switching interval.

The TRF2050's principle advantage is a result of the fractional-N mode capability. When operated in the fractional-N mode, the reference signal applied to the phase detector can be several times the channel spacing frequency of the wireless system. This enables the PLL loop filter bandwidth to be increased and thus allows the VCO to slew to new frequencies faster. The fractional "frequency" spurs which fall within the wireless system channel of interest are suppressed by fractional compensation circuitry and compensation charge pumps.

The TRF2050 also supports a SA7025 emulation mode which emulates the Philips SA7025 fractional-N synthesizer. The TRF2050 is available in a 20-pin plastic Shrink Small Outline Package (SSOP).




**Visit TI's RF web-site for more information on this or any other TI RF product. In addition to providing full descriptions of all of TI's RF products, this web-site provides:**

- Downloadable datasheets
- On-line EVM ordering
- On-line sample ordering
- RF training

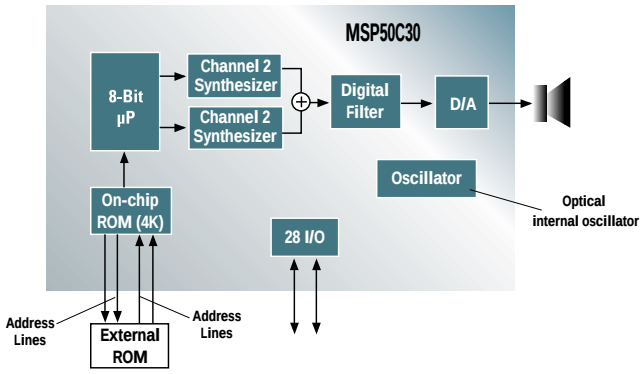
The URL for TI's RF web-site is: http://www.ti.com/sc/rf

■ **Check box 06** for a product bulletin.

SPEECH

# New external memory interface provides 8 hr. speech duration

**Key Applications:**
- Learning aids
- Talking books
- Games/toys
- Navigation systems
- Fitness equipment
- Warning systems
- Voice mailboxes




The MSP50C30 long duration speech processor features the same 8-bit microprocessor and dual synthesis channels found in the other MSP50C3X devices, with a 4K internal ROM, 1024 RAM locations, and 28 software-configurable I/O pins. This device contains 23 address and 8 data lines which allow a direct interface to external ROM (up to 8 Mbytes). With the external memory interface, the MSP50C30 is capable of long duration speech synthesis of up to 8 hours of LPC (Linear Predictive Coding).

The 28 I/O pins are configurable under software control to be either inputs or outputs. As inputs, they can be configured to be either high impedance or with a passive pull-up resistor. As outputs, they can be configured to be either totem pole or open drain. A special wake-up feature allows the device to be placed in a low power 'sleep' mode from which it will wake up upon a transition on any of 8 software definable pins.

A number of low bit-rate speech synthesis algorithms such as LPC, MELP (Mixed Excitation Linear Prediction), and CELP (Code Excited Linear Prediction) are available for use with the MSP50C30. These options provide great flexibility in the use of data space as well as the quality of the speech. Other options available for use with this device are ADPCM and FM Synthesis.

A number of mask options are available on the MSP50C30. These include DAC output options (two-pin digital or one-pin analog), a choice of an internal or external clock, and package type (die or 100-pin QFP).

Development tools available for supporting the MSP50C30 include an emulator and an assembler which are used in the code development process. These tools allow the user to compile, set breakpoints, single step through code, and examine/modify registers and memory in order to debug their code.

The following table lists the complete MSP50C3X family and the features for each device.

■ **Check box 07** for a datasheet.

**MSP50C3X Family of Synthesizers**

| | MSP50C30 | MSP50C32 | MSP50C33 | MSP50C34 | MSP50P34 | MSP50C37 | MSP50P37 |
|---|---|---|---|---|---|---|---|
| **ROM Type** | ROM | ROM | ROM | ROM | OTP | ROM | OTP |
| **ROM (bytes)** | 4K | 16K | 32K | 64K | 64K | 16K | 16K |
| **# of RAM locations** | 1024 | 256 | 256 | 256 | 256 | 256 | 256 |
| **I/O Pins (packaged)** | 28 | 10 | 10 | 10 | 10 | 18 | 18 |
| **I/O Pins (die)** | 28 | 10 | 10 | 24 | 24 | 18 | 18 |
| **A/D Input** | no | no | no | no | no | yes | yes |
| **Linear Amp** | no | no | no | no | no | yes | yes |
| **Pin Count (packaged)** | 100 | 16 | 16 | 16 | 16 | 28 | 28 |
| **Pin Count (die)** | 68 | 16 | 16 | 40 | 40 | 28 | 28 |

## Product Features

- External ROM interface (up to 8 Mbytes)
- Low bit rate synthesis algorithms (LPC, MELP, CELP)
- Internal clock generator
- Code execution from external memory
- Characterized for operation 0°C to 70°C

## Suggested resale price

**Quoted per device in minimum quantities of 25,000**

**MSP50C30:** $2.00

# TI Introduces New Information Service For Analog Engineers and Managers


Texas Instruments' new Sine-On service has arrived. Sine-On is a comprehensive service that will provide you with information and keep you up-to-date on TI's mixed signal and analog products based on your specific interests. All you have to do is tell us what product families you're interested in, and we'll take it from there. You see Sine-On offers you the ability to receive information on-line as well as in print form. It's entirely up to you!

Each edition of Sine-On highlights specific mixed signal and analog product families and is packed with design information on the latest products, sample packs, evaluation modules, application reports and more. At the back of each issue, customers will find easy-to-use selection guides and cross-reference information to make identifying the right devices for applications as painless as possible.

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# EVM KITS

Each EVM kit contains a fully-assembled evaluation board, data sheet, and a User's Guide for the evaluation board. Some kits also include applications notes, plus necessary software, cables and connectors.

**To order any of the EVM kits listed, please call our toll-free order desk number 1-800-477-8924 x 5800.**

| | | |
|---|---|---|
| TIR2000 | High-speed IrDA controller | $99.00 |
| TLC876/TLV876 | 10-bit, 20-MSPS ADC | $125.00 |
| TLC320AD50 | 16-bit sigma delta AIC | $75.00 |
| TLC320AD55 | 16-bit sigma delta AIC | $75.00 |
| TLC320AD56 | 16-bit sigma delta AIC | $75.00 |
| TLC320AD75C | ADA for digital audio applications | $500.00 |
| TPS2014 | PCMCIA distribution switch | $0.00 |
| TPS9104 | Cellphone P/S with audio PAs | $50.00 |
| TPS6735 | 5 V, 200 mA inverting dc-dc converter | $50.00 |
| TLC5510 | 8-bit, 20 MSPS ADC | $50.00 |
| TLC5540 | 8-bit, 40 MSPS ADC | $50.00 |
| TLC2543 | 5 V, 12-bit ADC | $75.00 |
| TLV2543 | 3 V, 12-bit ADC | $75.00 |
| TLC2932 | 50 MHz Phase Lock Loop | $85.00 |
| TSL230 | Light-to-frequency converter | $89.95 |
| PC404-13 (TSL213) | 200 DPI linear array | $124.95 |
| TSL215 | 200 DPI linear array | $127.95 |
| PC404-401 (TSL401) | 400 DPI linear array | $124.95 |
| PC404-1401 (TSL1401) | 400 DPI linear array | $124.95 |
| PC404-1402 (TSL1402) | 400 DPI linear array | $127.95 |
| Audio amps | Audio power amp Plug-n-Play (basekit) | $150.00 |
| TMS320C5x | C5xDSP DSK | $99.00 |
| TSBKBACKPL | Backplane card | $2000.00 |
| TSBKPCITST | PCILynx™ and 200 Mbps phy – feature rich board | $1000.00 |
| TSBKPCI | PCILynx™ and 200 Mbps phy – value board | $275.00 |
| TSBKGPCILYNX | TSB12LV31/TSB21LV03 peripheral kit | $1000.00 |
| TSBKPRPHRL | Peripheral Card | $1000.00 |
| TUSBK4HUB | 4-Port stand-alone hub kit | $349.00 |
| TUSBK7HUB | 7-Port stand-alone hub kit | $399.00 |

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