Chapter 3
Background

This chapter presents a brief description of the background of the Universal Serial Bus including design goals, features of the bus, and existing technologies.

3.1 Goals for the Universal Serial Bus

The Universal Serial Bus is specified to be an industry standard extension to the PC architecture with a focus on Computer Telephony Integration (CTI), consumer, and productivity applications. The following criteria were applied in defining the architecture for the Universal Serial Bus:

- Ease of use for PC peripheral expansion
- Low-cost solution that supports transfer rates up to 12 Mbs
- Full support for the real-time data for voice, audio, and compressed video
- Protocol flexibility for mixed-mode isochronous data transfers and asynchronous messaging
- Integration in commodity device technology
- Comprehend various PC configurations and form factors
- Provide a standard interface capable of quick diffusion into product
- Enable new classes of devices that augment the PC's capability

3.2 Taxonomy of Application Space

Figure 3-1 describes a taxonomy for the range of data traffic workloads that can be serviced over a Universal Serial Bus. As can be seen, a 12 Mbs bus comprehends the mid-speed and low-speed data ranges. Typically, mid-speed data types are isochronous and low-speed data comes from interactive devices. The Universal Serial Bus being proposed is primarily a desktop bus but can be readily applied to the mobile environment. The software architecture allows for future extension of the Universal Serial Bus by providing support for multiple Universal Serial Bus host controllers.

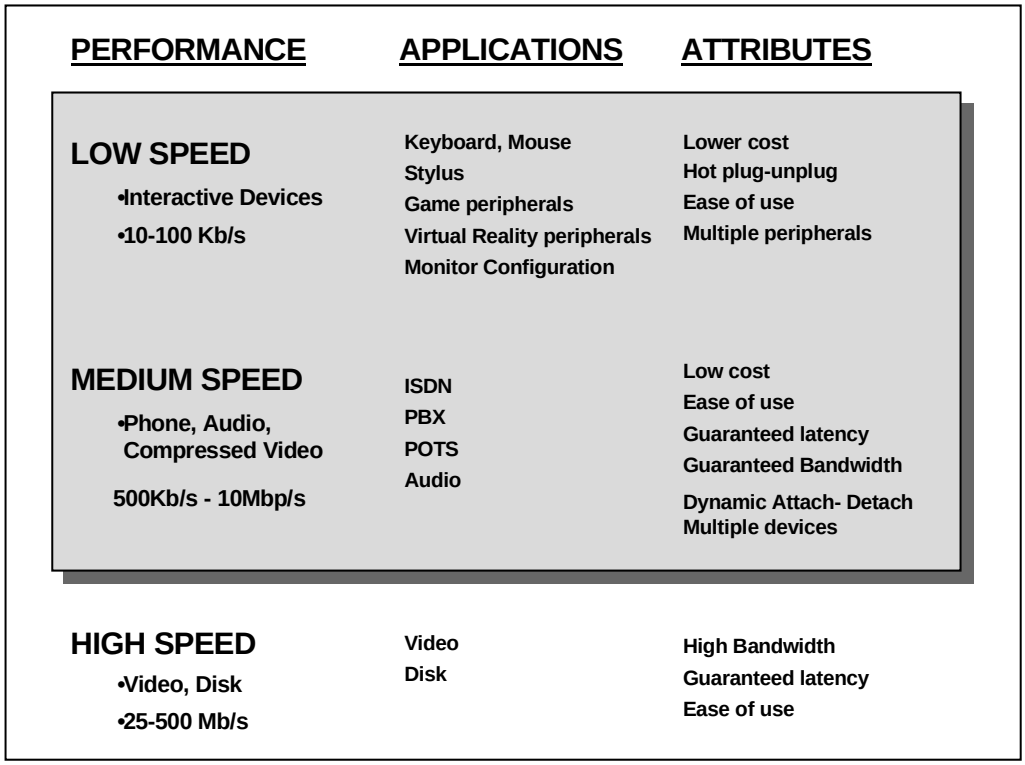

Figure 3-1. Application Space Taxonomy

3.3 Feature List

The Universal Serial Bus specification provides a selection of attributes that can achieve multiple price-performance integration points and can enable functions that allow differentiation at the system and component level. Features are categorized by benefits below:

Easy to use for end user

- Single model for cabling and connectors
- Electrical details isolated from end user; e.g., bus terminations
- Self identifying peripherals, automatic mapping of function to driver, and configuration
- Dynamically attachable and reconfigurable peripherals

Wide range of workloads and applications

- Suitable for device bandwidths ranging from a few kbs to several Mbs
- Supports isochronous as well as asynchronous transfer types over the same set of wires
- Multiple Connections: Support for concurrent operation of many devices
- Support for up to 127 physical devices
- Supports transfer of multiple data and message streams between the host and devices
- Allows compound devices; i.e., peripherals composed of many functions
- Lower protocol overhead resulting in high bus utilization

Isochronous bandwidth

- Guaranteed bandwidth and low latencies appropriate for telephony, audio, etc.
- Isochronous workload may use entire bus bandwidth

Flexibility

- Wide range of packet sizes, allowing a range of device buffering options
- Wide range of device data rates by accommodating packet buffer size and latencies
- Flow control for buffer handling built into protocol

Robustness

- Error handling/fault recovery mechanism built into protocol
- Dynamic insertion and removal of devices identified in user perceived real-time
- Support for identification of faulty devices

Synergy with PC industry

- Simple protocol to implement and integrate
- Consistent with the PC Plug and Play architecture
- Leverages existing operating system interfaces

Low-cost implementation

- Low cost sub channel at 1.5 Mbs
- Optimized for integration in peripheral and host hardware
- Suitable for development of low cost peripherals
- Low cost cables and connectors
- Utilizes commodity technologies

Upgrade path

- Architecture upgradeable to support multiple Universal Serial Bus host controllers in a system

3.4 Some Existing Technologies

There are several technologies that are commonly considered to be serial buses. Each of these buses were defined for a specific range of application(s). A few of them are listed below:

- **Apple desktop bus (ADB)**
  This is a proprietary minimalist serial interface that provides a simple read/write protocol to up to 16 devices. The cost of hardware interface is estimated to be very low. The ADB supports data rates up to 90 kbs, just enough to communicate with keyboards, pointing devices, or other desktop I/O devices.

- **Access.bus (A.b)**
  The Access.bus is being developed by the Access.bus Industry Group, based on the Philips I^2C technology and a DEC software model. The application space for the Access.bus is primarily keyboards and pointing devices; however, A.b is more versatile then the ADB. The protocol has well defined specifications for the dynamic attach, arbitration, data packets, configuration, and software interface. While addressing is provided for up to 127 devices, the practical loading is limited by cable lengths and power distribution considerations. Revision 2.2 of the A.b specification specifies the bus for 100 kbs operation, but the technology has headroom to go up to 400 kbs using the same separate clock and data wires.

- **IEEE P1394**
  The IEEE P1394 is a high performance serial bus. The application space for P1394 is primarily hard disk and video peripherals, which may require bus bandwidth in excess of 100 Mbs. The protocol supports both isochronous and asynchronous transfers over the same set of four signal wires, broken up as differential pair of clock and data signals. The P1394 specification is very well defined and the first generation devices, based on the IEEE specification, are just coming to market. Current pricing of P1394 solutions is considered competitive relative to SCSI disk interfaces, but not for generic desktop connectivity.

- **CHI**
  The Concentration Highway Interface (CHI) was developed by AT&T for terminals and digital switches. CHI is a full duplex time division multiplexed serial interface for digitized voice transfers in communications systems. The protocol consists of a number of fixed time slots that can carry voice data and control information. The current specification supports data transfer rates up to 4.096 Mbs. The CHI bus has four signal wires: Clock, Framing, Receive data, and Transmit data. Both, the Framing and the Clock signals are generated centrally (i.e., PBX switch).

- **GeoPort**
  The GeoPort was originally developed by Apple Computer, Inc. to primarily enable Macintosh telephony applications. Current specification of the GeoPort supports data transfer rates up to 2 Mbs and provides point to point connectivity over a radius of 4 ft. The standard GeoPort specifies a 9-pin connector (8 pins and an optional 9th power pin) and uses RS-422 signaling. Additionally, Apple has defined an alternate 14-pin connector for extended cable lengths. The GeoPort protocol provides three different operating modes: Beaconing, TDM, and Packetized transfer modes. Apple is currently licensing the GeoPort specification.