Chapter 7
Electrical

This chapter describes the electrical specification for the USB. It contains signaling, power distribution, and physical layer specifications.

7.1 Signaling

The signaling specification for the USB is described in the following subsections.

7.1.1 USB Driver Characteristics

The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the V_{OL} of 0.3 V with a 1.5 kΩ load to 3.6 V and in its high state must be above the V_{OH} of 2.8 V with a 15 kΩ load to ground as listed in Table 7-4. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate voltage the signal pins of -0.5 V to 3.8 V with respect to its local ground reference without damage. It must tolerate this voltage for 10.0 μs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state.

7.1.1.1 Full Speed (12 Mbs) Driver Characteristics

A full speed USB connection is made through a shielded, twisted pair cable with a characteristic impedance (Z_0) of 90 Ω ±15% and a maximum length of 5 meters. The impedance of each of the drivers must be between 29 Ω and 44 Ω. The data line rise and fall times must be between 4 ns and 20 ns, smoothly rising or falling (monotonic), and be well matched to minimize RFI emissions and signal skew.

For a CMOS implementation, the driver impedance will typically be realized by a CMOS driver with an impedance significantly less than this resistance with a discrete series resistor making up the balance. Figure 7-1 shows an example of how a full speed driver might be done using two identical CMOS buffers which have an output impedance between 3 Ω and 15 Ω, and two series resistors of 27 Ω. Figure 7-2 shows the full speed driver signal waveforms.
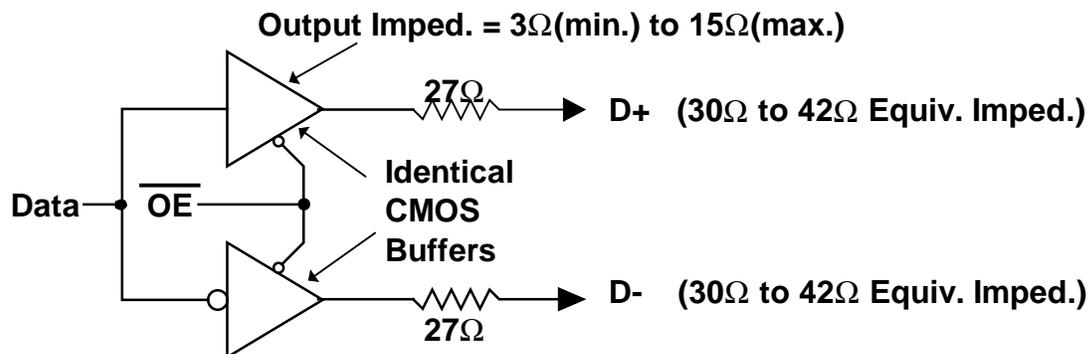

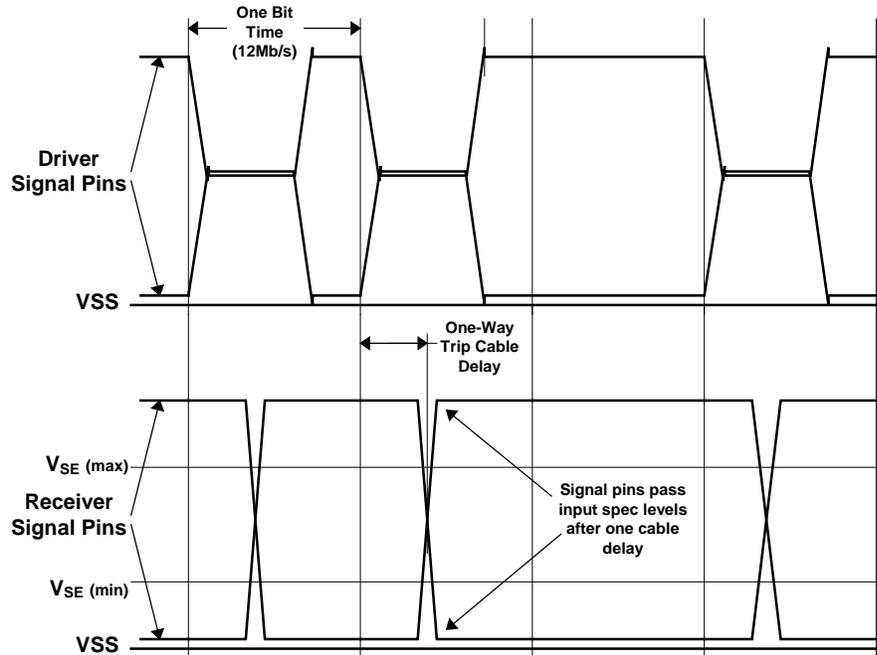**Figure 7-1. Example Full Speed CMOS Driver Circuit**

Figure 7-2. Full Speed Driver Signal Waveforms

7.1.1.2 Low Speed (1.5 Mbs) Driver Characteristics

A low speed USB connection is made through an unshielded, untwisted wire cable, a maximum of 3 meters in length. The rise and fall time of the signals on this cable must be greater than 75 ns to keep RFI emissions under FCC class B limits, and less than 300 ns to limit timing delays and signaling skews and distortions. The driver must reach the specified static signal levels with smooth rise and fall times, and minimal reflections and ringing when driving the cable (see Figure 7-3). This cable and driver are used only on network segments between low speed devices and the ports to which they are connected.
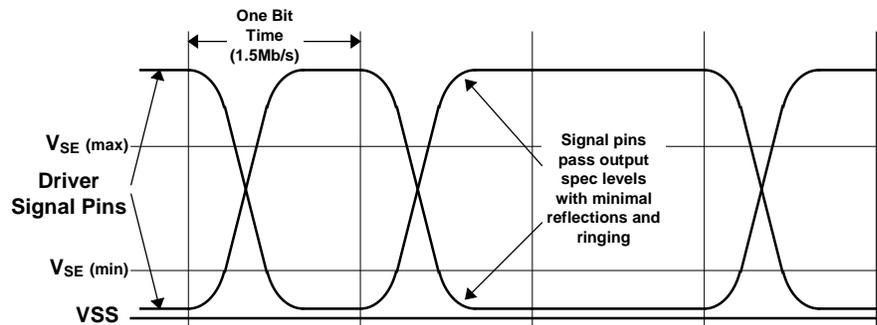

Figure 7-3. Low Speed Driver Signal Waveforms

7.1.1.3 Driver Usage

Full speed buffers are used on the upstream ports (towards the host) of all hubs and full speed functions. All devices with hubs must be full speed devices. A full speed driver will be used to send data at both and low speed data rates. However, the signaling always uses full speed signaling conventions (refer to Table 7-1) and edge rates. Running at low speed data rates does not change the driver's characteristics.

Low speed buffers are used on the upstream ports of low speed functions. The downstream ports of all hubs (including the host) are required to be capable of both driver characteristics, such that any type of device

can be plugged in to these ports (see Figure 7-5 and Figure 7-6). Low speed drivers only send at the low speed data rate using low speed signaling conventions (refer to Table 7-1) and edge rates.

7.1.2 Receiver Characteristics

A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 7-4. The receiver must tolerate static input voltages between -0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. They must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise.
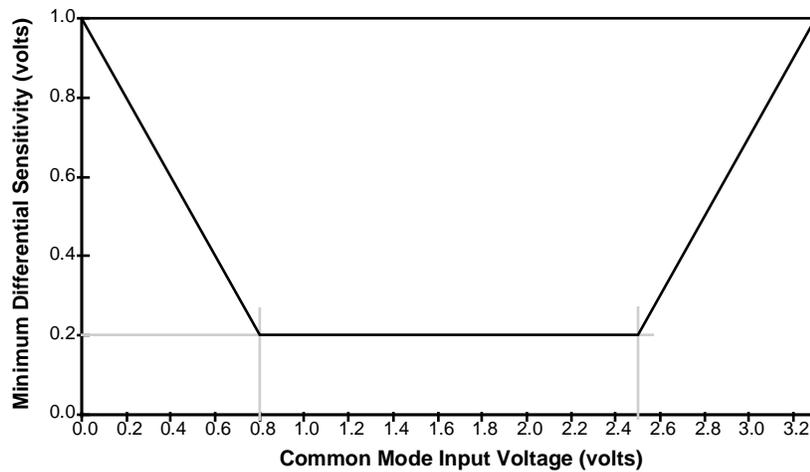

Figure 7-4. Differential Input Sensitivity Over Entire Common Mode Range

7.1.3 Signal Termination

The USB is terminated at the hub and function ends as shown below. Full speed and low speed devices are differentiated by the position of the pull-up resistor on the downstream end of the cable. Full speed (F.S.) devices are terminated as shown in Figure 7-5 with the pull-up on the D+ line. Low speed (L.S.) devices are terminated as shown in Figure 7-6 with the pull-up on the D- line.

The pull-up terminator is a 1.5 kΩ ±5% resistor tied to a voltage source between 3.0 V and 3.6 V referenced to the local ground. The pulldown terminators are resistors of 15 kΩ ±5% connected to their local ground.
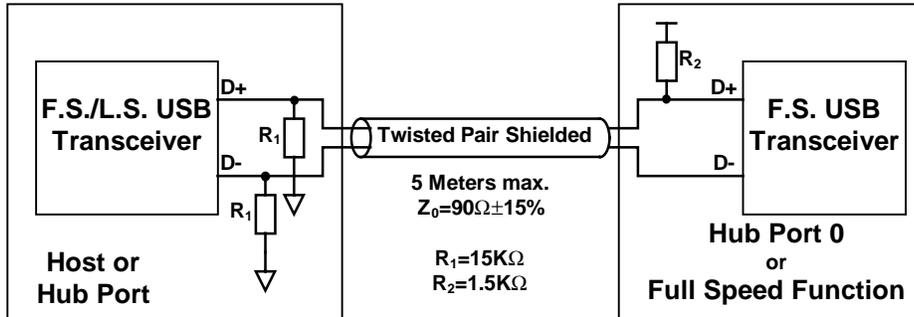
Figure 7-5. Full Speed Device Cable and Resistor Connections
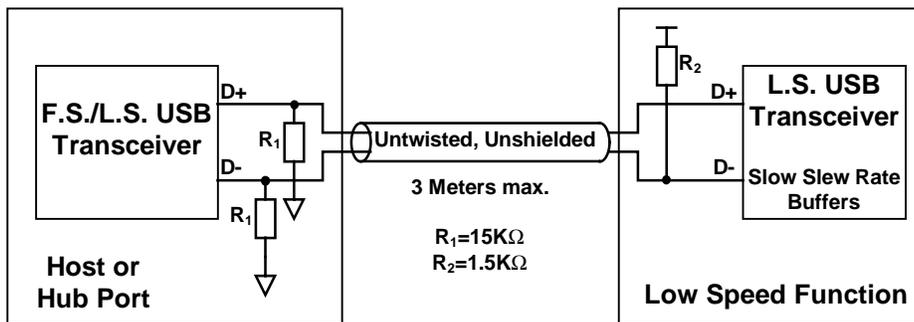
Figure 7-6. Low Speed Device Cable and Resistor Connections

7.1.4 Signaling Levels

Table 7-1 shows a summary of the USB signaling levels. The signaling levels are described below and in the following sections.

Table 7-1. Signaling Levels

Bus State	Signaling Levels	
	From Originating Driver	**At Receiver**
Differential "1"	(D+) - (D-) > 200 mV and D+ or D- > V_{SE} (min.)	
Differential "0"	(D+) - (D-) < -200 mV and D+ or D- > V_{SE} (min.)	
Data 'J' State: Low Speed Full Speed	 Differential "0" Differential "1"	
Data 'K' State: Low Speed Full Speed	 Differential "1" Differential "0"	
Idle State: Low Speed Full Speed	 Differential "0" and D- > V_{SE} (max.) and D+ < V_{SE} (min.) Differential "1" and D+ > V_{SE} (max.) and D- < V_{SE} (min.)	
Resume State: Low Speed Full Speed	 Differential "1" and D+ > V_{SE} (max.) and D- < V_{SE} (min.) Differential "0" and D- > V_{SE} (max.) and D+ < V_{SE} (min.)	
Start of Packet (SOP)	Data lines switch from Idle to 'K' State	
End of Packet (EOP)	D+ and D- < V_{SE} (min) for 2 bit times[1] followed by an Idle for 1 bit time	D+ and D- < V_{SE}(min) for ≥ 1 bit time[2] followed by a 'J' State
Disconnect (Upstream only)	(n.a.)	D+ and D- < V_{SE}(max) for ≥ 2.5 μs
Connect (Upstream only)	(n.a.)	D+ or D- > V_{SE}(max) for ≥ 2.5 μs
Reset (Downstream only)	D+ and D- < V_{SE} for ≥10 ms	D+ and D- < V_{SE} (min)for ≥ 2.5 μs (must be recognized by 5.5 μs)[3]

Note 1: The width of EOP is defined in bit times relative to the speed of transmission.

Note 2: The width of EOP is defined in bit times relative to the device type receiving the EOP.

Note 3: These times apply to an active device that is not in the suspend state.

The 'J' and 'K' data states are the two logical levels used to communicate differential data in the system. Differential signaling is measured from the point where the data line signals cross over. Differential data signaling is not concerned with the level at which the signals cross, as long as it is within the common mode range. When the bus is not in the differential signaling mode, the data lines have to be outside the VSE switching threshold range to be valid, as in the idle and resume states. Note that the idle and resume states are logically equivalent to the 'J' and 'K' states respectively.

Table 7-1 shows the 'J' and 'K' states for a full speed to be inverted from those of low speed. The sense of data, idle, and resume signaling is set by the type of device that is being attached to a port. If a full speed device is attached to a port, that segment of the USB network uses full speed signaling conventions (and fast rise and fall times) even if the data being sent across the data lines is at the low speed data rate. The low speed signaling conventions shown in Table 7-1 (plus slow rise and fall times) are only used between a low speed device and the port to which it is attached. The method of determining the device type, and, therefore, the signaling convention used, is described in the next section.

7.1.4.1 Connect and Disconnect Signaling

All ports on the downstream side of the host or a hub have pull-down resistors on both the D+ and D- lines. All devices have a pull-up resistor on one of the data lines on their upstream port. The type of device determines which data line has the pull-up resistor. Full speed devices have the pull-up on the D+ line (see Figure 7-5) and low speed devices have the pull-up on the D- line (see Figure 7-6). When a device is attached to hub or host but the data lines are not being driven, these resistors create a quiescent bias condition on the lines such that the data line with the pull-up is above 2.8 V and the other data line is near ground. This is called the idle state.

When no function is attached to the downstream port of the host or hub or the pull-up resistor on an attached device is not powered, the pull-down resistors will cause both D+ and D- to be pulled below the single-ended low threshold of the host or hub port. This creates a state called a single-ended zero (SE0) on the downstream port. A disconnect condition is indicated if an SE0 persists on a downstream port for more than 2.5 µs (30 full speed bit times). Note that disconnect signaling applies only in an upstream direction (see Figure 7-7).

A connect condition will be detected when a device is connected to the host or hub's port, and one of the data lines is pulled above the single-ended high threshold level for more than 2.5 µs (30 full speed data bit times). The data line that is high when the port state changes from disconnected to connected sets the idle state for this bus segment and determines whether the connected device is a full speed device or a low speed device. All signaling levels given in Table 7-1 are set for this network segment (and this segment alone) once the idle state is determined. Figure 7-8 shows a full speed device connection sequence and Figure 7-9 shows a low speed device connection sequence.

All hub ports start out in an implied disconnected state after power is applied to that port. If a device is connected to the port, the port goes through the connect sequence described above to detect the device type and set the port signaling characteristics. (Refer to Section 11.2.3.)
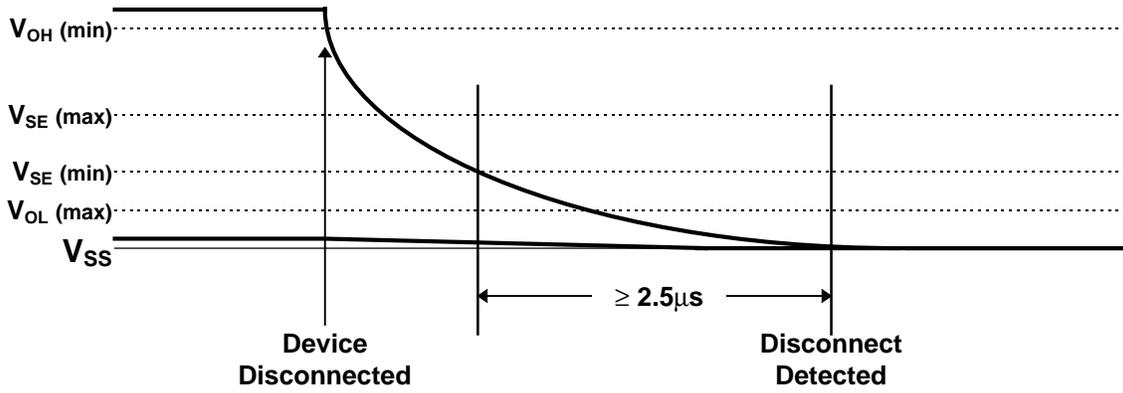
V_{OH} (min)
V_{SE} (max)
V_{SE} (min)
V_{OL} (max)
V_{SS}

$\geq 2.5\mu s$

**Device
Disconnected**

**Disconnect
Detected**

Figure 7-7. Disconnect Detection

V_{OH} (min)
V_{SE} (max)
V_{SE} (min)
V_{OL} (max)
V_{SS}

D+

D-

$\geq 2.5\mu s$

**Device
Connected**
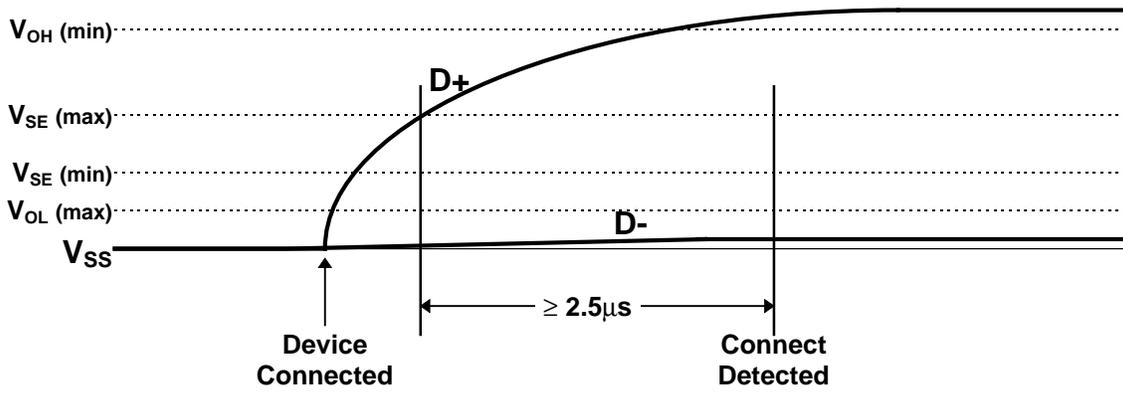
**Connect
Detected**

Figure 7-8. Full Speed Device Connect Detection

V_{OH} (min)
V_{SE} (max)
V_{SE} (min)
V_{OL} (max)
V_{SS}

D-

D+

$\geq 2.5\mu s$

**Device
Connected**
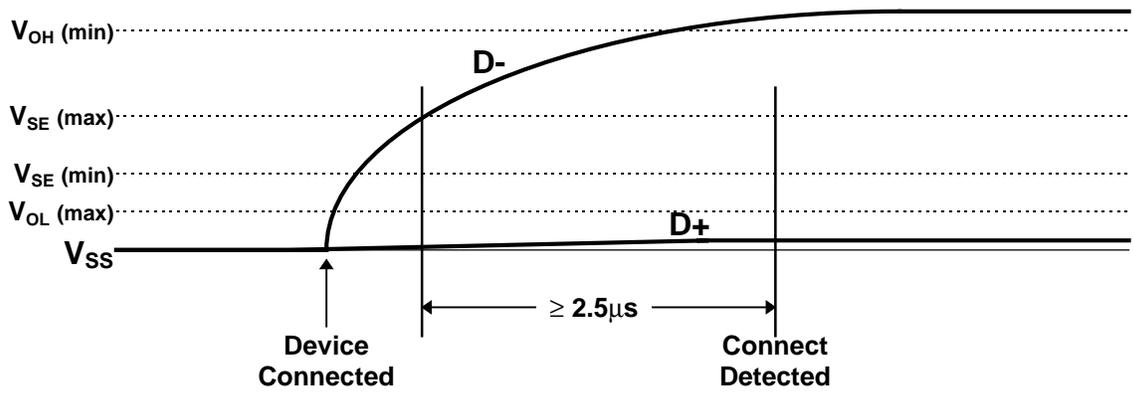
**Connect
Detected**

Figure 7-9. Low Speed Device Connect Detection

7.1.4.2 Data Signaling

Data transmission within a packet is done with differential signals. A differential 1 on the bus is represented by D+ being at least 200 mV more positive than D- as seen at the receiver, and a differential 0 is represented by D- being at least 200 mV more positive than D+ as seen at the receiver. The signal cross over point must be between 1.3 V and 2.0 V.

The start of a packet (SOP) is signaled by the originating port by driving the D+ and D- lines from the idle state to the opposite logic level ('K' state). This switch in levels represents the first bit of the Sync field. Hubs must limit the distortion of the width of the first bit after SOP when it is retransmitted to less than 5 ns. Distortion can be minimized by matching the nominal data delay through the hub with the output enable delay of the hub.

The single-ended 0 state is used to signal an end of packet (EOP). The single-ended 0 state is indicated by both D+ and D- being below 0.8 V. EOP will be signaled by driving D+ and D- to the single-ended 0 state for two bit times followed by driving the lines to the idle state for one bit time. The transition from the single-ended 0 to the idle state defines the end of the packet. The idle state is asserted for 1 bit time and then both the D+ and D- output drivers are placed in their high-impedance state. The bus termination resistors hold the bus in the idle state. Figure 7-10 shows the signaling for start and end of a packet.
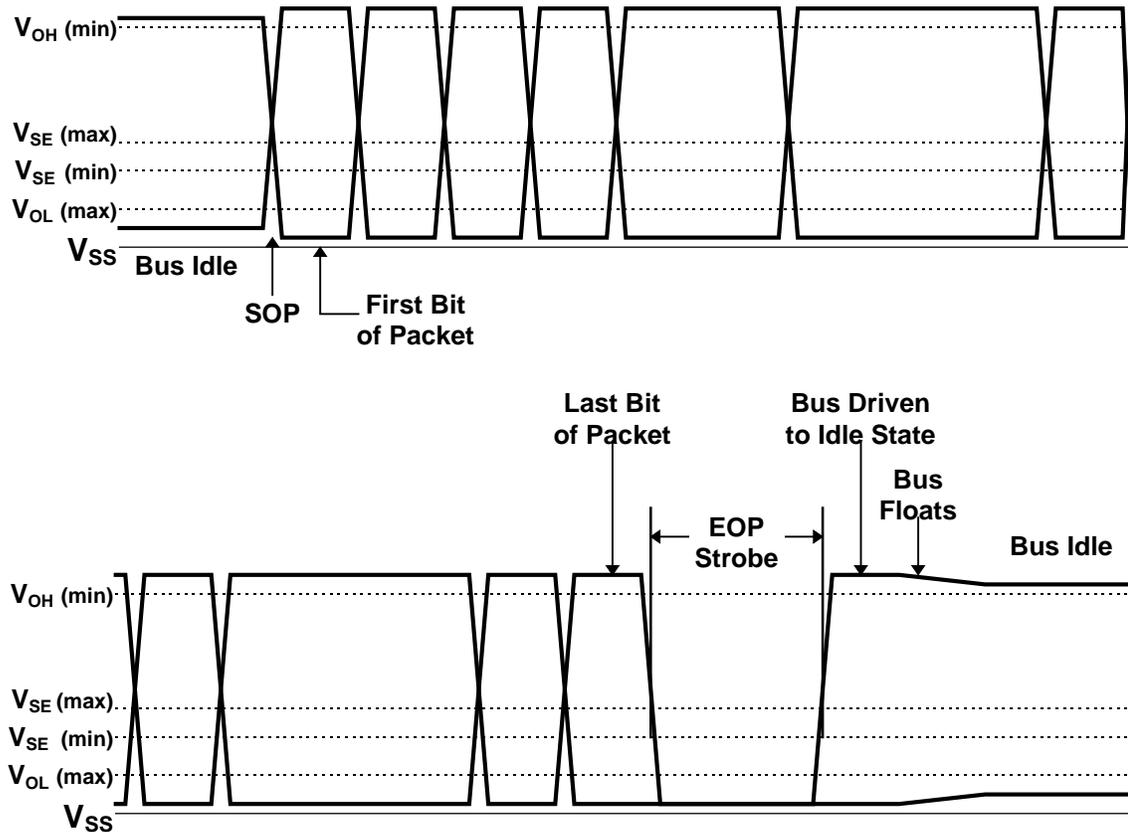

Figure 7-10. Packet Transaction Voltage Levels

7.1.4.3 Reset Signaling

A reset is signaled downstream from a hub port on the bus by the presence of an extended SE0 at the upstream port of a device. After the reset is removed, the device will be in the attached, but not yet addressed or configured state (refer to Section 9.2). Note that reset signaling applies only in the downstream direction.

The reset signal can be generated by host command on any hub or host controller port. The reset signal must be generated for a minimum of 10 ms. The port that generated the reset will be sent to the logically disconnected state at the end of the reset. If a device is connected to the port, the bus pull-up resistor will determine the device type (low or full speed) and the port will end up in the disabled state (refer to Section 11.2.3).

An active device (powered and not in the suspend state) seeing a single-ended zero on its upstream port for more than 2.5 µs may treat that signal as a reset, but must have interpreted the signaling as a reset within 5.5 µs. A device that recognizes a reset from a SE0 between 32 and 64 full speed bit times or between 4 and 8 low speed bit times satisfies these requirements. The reset signal propagates through all enabled ports of any hubs downstream of the signaling port, but does not propagate through any ports that are disabled. A bus-powered hub that receives a reset on its root port removes power from all its downstream ports. After the reset is removed, all devices that received the reset are set to their default USB address and are in the unconfigured state. All ports on a hub that received a reset are disabled.

Hubs must be able to establish connectivity, and all devices must be able to accept device address via a SET_ADDRESS command (refer to Section 9.5) no later than 10 ms after the reset is removed. Failure to establish connectivity or accept an address may cause the device not to be recognized by the USB enumerator. In the case of a hub, it may also cause any devices connected to that hub not to be recognized. All other requests for data or service, except SETUP packets (refer to Section 8.4.5.4), can be NAKed for a period up to 5.0 seconds after which the device is declared defective and is not recognized.

Reset can wake a device from the suspended mode. It is recommended that the device wait for its clocks to stabilize before accepting the reset to avoid spurious single-ended zero events from causing the device to reset. A device may take up to 10 ms to wake up from the suspended state.

7.1.4.4 Suspending

All devices must support the suspend mode. They can go into the suspended mode from any powered state. They go into the suspend state when they see a constant idle state on their bus lines for more than 3.0 ms. Any bus activity will keep a device out of the suspend state. The SOF packet (refer to Section 8.4.2) is guaranteed to occur once a frame to keep full speed devices awake during normal bus operation. Hubs that are not in the suspend state keep low speed devices awake by generating a low speed EOP on enabled ports that are attached to low speed devices (refer to Section 11.2.5.1). When a device is in the suspend state, it draws less than 500 µA from the bus.

All devices can be awakened from the suspend state by switching the bus state to the resume state, by normal bus activity, or by signaling a reset. Some devices have the ability to be awakened by actions associated with their internal functions and then cause signaling on their upstream connection to wake or alert the rest of the system. This feature is called remote wake-up and is described in Section 7.1.4.5.

7.1.4.4.1 Global Suspend

Global suspend is used when no communication is desired anywhere on the bus and the whole network is placed in the suspend state. The host signals the start of suspend by ceasing all its transmissions (including the SOF token). As each device on the bus recognizes the lack of activity, and that the bus is in the idle state for the appropriate length of time, it goes into its suspend state. As hubs go into the suspended state, they cease to send the low speed EOP on any downstream low-speed configured ports.

7.1.4.4.2 Selective Suspend

The system software may want to conserve power by suspending only certain segments of the topology, while continuing regular operation on the remaining segments. Segments of the network can be selectively put into the suspend state by suspending the hub port to which that segment is attached. The suspended port will block activity to this segment of the bus and the attached devices will go into suspend after the appropriate delay as described above.

Any non-hub device can be suspended in this way. Any hub not involved in connecting the remaining devices to the host may also be suspended by disabling the port to which it is attached. Devices that are selectively suspended can still alert the system with a remote wake-up signaling, although the process is slightly different. A description of the suspend port state can be found in Section 11.2.3 and selective suspend is further described in Section 11.5.2.

7.1.4.5 Resume

Once a device is in the suspend state, its operation can be resumed by receiving non-idle signaling on the bus, or it can signal the system to resume operation if it has the remote wake-up capability. The resume signaling state is used by the host or a device with remote wake-up to awaken the system. Hubs play an important role in the propagation and generation of resume signaling. The following description is an outline of a general global resume sequence. A complete description of the resume sequence, the special cases caused by selective suspend, and the role of the hub is given in Section 11.5.

The host may signal resume anytime after it places the bus into the suspend mode. It must send the resume signaling for at least 20 ms and then end the resume signaling with a standard low speed EOP (two low speed bit times of SE0 followed by a transition to the idle state). The 20 ms of resume signaling insures that all devices in the network that are enabled to see the resume are awakened. The EOP tears down the connectivity established by the resume signaling and prepares the hubs for normal operation. After resuming the bus, the host must begin sending bus traffic (at least the SOF token) within 3 ms to keep the system from going back into the suspend state.

A device with remote wake-up capability must wait for at least 5 ms after the bus is in the idle state before sending the remote wake-up resume signaling. This allows the hubs to get into their suspend state and prepare for propagating resume signaling. The remote wake-up device must hold the resume signaling for at least 10 ms and no more than 15 ms. At the end of the resume signaling, the device puts its data lines into the high impedance state.

The hub upstream of the remote wake-up device will propagate the resume signaling to its root port and all of its enabled downstream ports, including the port which originally signaled the resume. The hub must begin this rebroadcast of the resume signaling within 50 µs of receiving the original resume. The resume signal will propagate in this manner upstream until it reaches the host (or a suspended hub port - refer to Section 11.5.2.1) which will reflect the resume downstream on its enabled ports, as in any other hub. Meanwhile, the hubs that transported the resume to the host wake up within 10 ms. After a 1 ms delay, they reverse the direction of connectivity in their root port from upstream to downstream and reflect the signal state on the root port onto their enabled downstream ports. This puts the host in control of the resume signaling which then proceeds as described above.

Port connects and disconnects can also cause the affected hub to send a resume signal and awaken the system. Refer to Section 11.5 for more details.

(Note that the host can wake up the entire bus by resetting it. This requires that the entire bus must be re-enumerated and reconfigured.)

7.1.5 Data Encoding/Decoding

The USB employs NRZI data encoding when transmitting packets. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. Figure 7-11 shows a data stream and the NRZI equivalent and Figure 7-12 is a flow diagram for NRZI. The high level represents the 'J' state on the data lines in this and subsequent figures showing NRZI encoding. A string of zeros causes the NRZI data to toggle each bit time. A string of ones causes long periods with no transitions in the data.
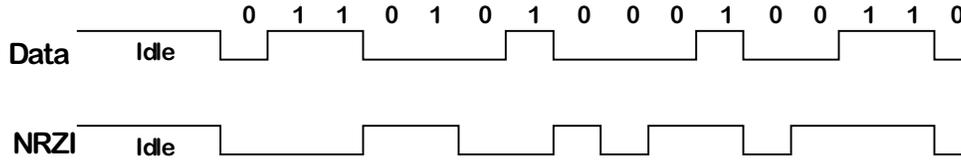
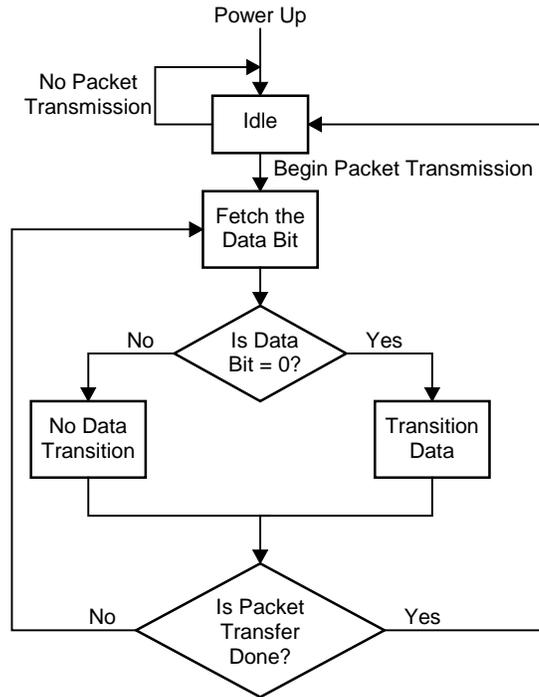**Figure 7-11. NRZI Data Encoding**

Figure 7-12. Flow Diagram for NRZI

7.1.6 Bit Stuffing

In order to ensure adequate signal transitions, bit stuffing is employed by the transmitting device when sending a packet on the USB (see Figure 7-13 and Figure 7-14). A 0 is inserted after every six consecutive 1's in the data stream before the data is NRZI encoded to force a transition in the NRZI data stream. This gives the receiver logic a data transition at least once every seven bit times to guarantee the data and clock lock. The receiver must decode the NRZI data, recognize the stuffed bits, and discard them. Bit stuffing is enabled beginning with the Sync Pattern and throughout the entire transmission. The data "one" that ends the Sync Pattern is counted as the first one in a sequence. Bit stuffing is always enforced, without exception. If required by the bit stuffing rules, a zero bit will be inserted even if it is the last bit before the end-of-packet (EOP) signal.
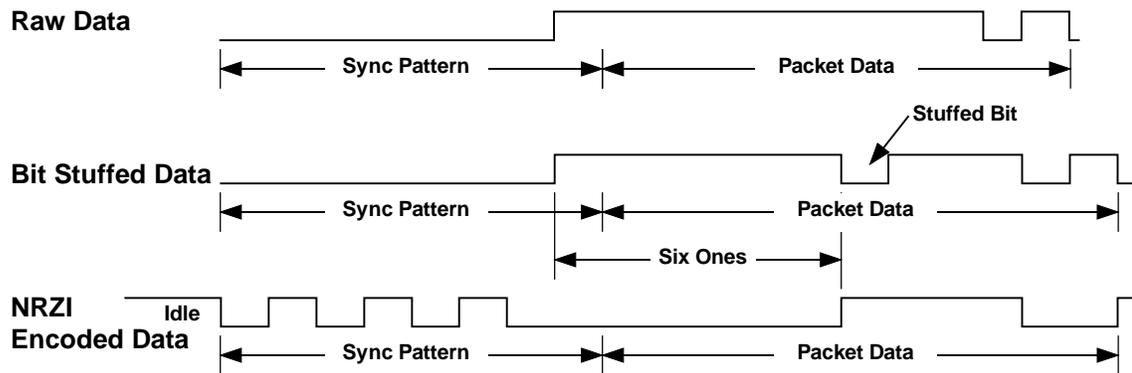
<u>Data Encoding Sequence:</u>
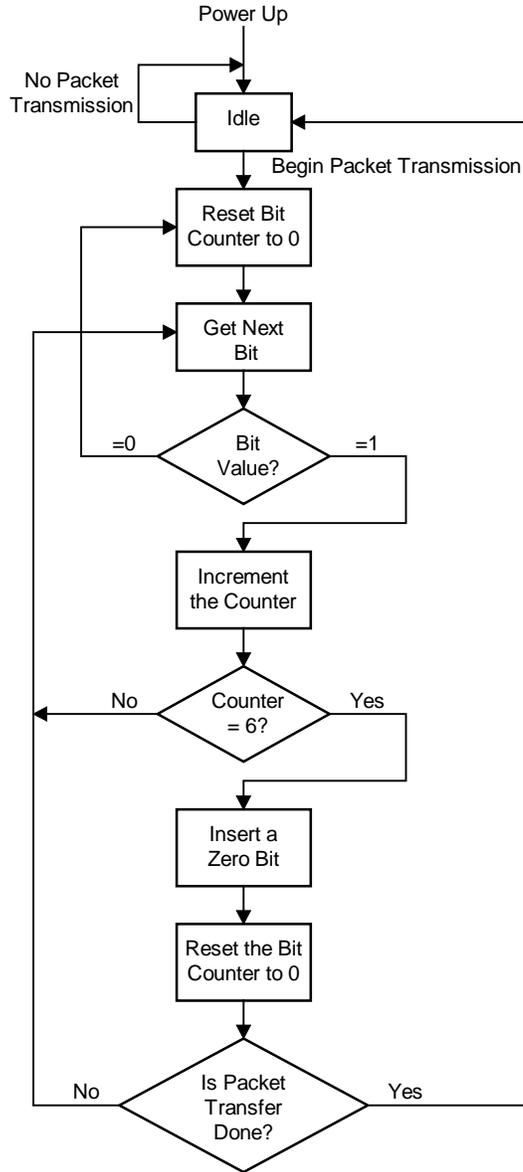
Figure 7-13. Bit Stuffing

Figure 7-14. Flow Diagram for Bit Stuffing

7.1.7 Sync Pattern

The NRZI bit pattern shown in Figure 7-15 is used as a synchronization pattern and is prefixed to each packet. This pattern is equivalent to a data pattern of seven 0's followed by a 1 (0x80).
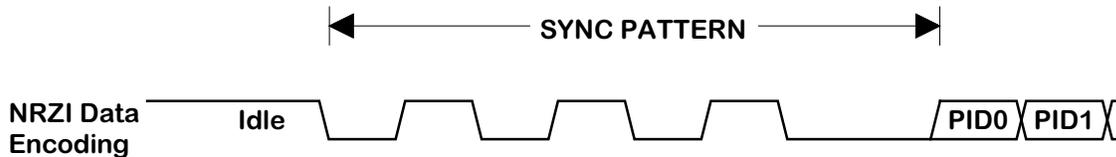
Figure 7-15. Sync Pattern

7.1.8 Initial Frame Interval and Frame Adjustability

The USB defines a frame interval to be 1.000 ms long. The frame interval is measured from the start of the Start of Frame (SOF) PID in one frame to the same point in the SOF token of the next frame. The permitted tolerance on the initial frame interval is ±0.05% (500 ppm). This tolerance includes inaccuracies from all sources: initial frequency accuracy, crystal capacitive loading, supply voltage on the oscillator, temperature, and aging.

The host controller must be able to adjust the frame interval. There are two possible components to the frame interval adjustability. If the host's data rate clock is not exactly 12.00 Mbs, then the initial ±0.05% frame interval accuracy can be met by changing the default number of bits per frame from the nominal of 12,000. (A host controller component, that has a range of possible clock source values, may have to make this initial frame count a programmable value. The range of these values is given in Section 7.1.9.) An additional adjustability of ±15 full speed bit times is required to allow the host to synchronize to an external time reference. The frame interval can be reprogrammed by no more than one full speed bit time each adjustment during normal bus operation.

Hubs and certain full speed functions need to track the frame interval. They also are required to have sufficient frame timing adjustability to compensate for its own frequency tolerance and track the host's ±15 full speed bit time adjustability range.

7.1.9 Data Signaling Rate

The full speed data rate is nominally 12 Mbs. The data rate tolerance for host, hub, and full speed functions is ±0.25% (2500 ppm). The accuracy of the host controller's data rate must be known to better than ±0.05% (500 ppm) in order to meet the frame interval accuracy. This tolerance includes inaccuracies from all sources: initial frequency accuracy, crystal capacitive loading, supply voltage on the oscillator, temperature, and aging.

The low speed data rate is nominally 1.5 Mbs. The permitted frequency tolerance for low speed functions is ±1.5% (15000 ppm). This tolerance includes inaccuracies from all sources: initial frequency accuracy, crystal capacitive loading, supply voltage on the oscillator, temperature, and aging. The jitter in the low speed data rate must be less than 10 ns. This tolerance allows the use of resonators in low cost, low speed devices

7.1.10 Data Signal Rise and Fall Time

The output rise time and fall time are measured between 10% and 90% of the signal (see Figure 7-16). Edge transition time for the rising and falling edges of full speed data signals is 4 ns (minimum) and 20 ns (maximum) measured with a capacitive load (C_L) of 50 pF. The rise and fall times must be well matched. The rise and fall time of low speed signals is 75 ns (minimum) into a load of 50 pF and 300 ns (maximum) into a capacitive load of 350 pF. In both cases, the rising and falling edges should be smoothly transitioning (monotonic) when driving their respective cables to avoid excessive EMI. (In full speed signaling, the driver and cable impedances are not matched, so reflections from the receiver end of the cable are expected.)
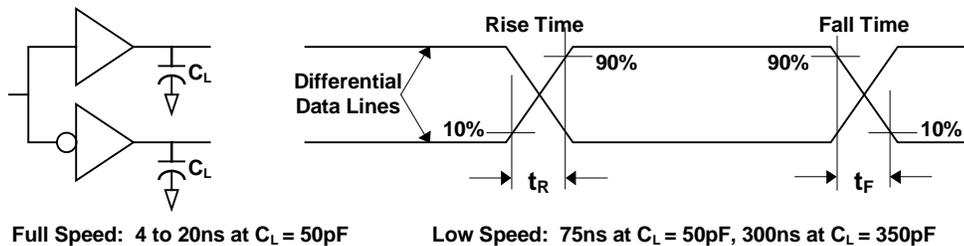

Figure 7-16. Data Signal Rise and Fall Time

7.1.11 Data Source Signaling

This section covers the timing characteristics of data produced and sent from a device (the data source). Section 7.1.12 covers the timing characteristics of data that is transmitted through the repeater section of a hub. In this section, T_{PERIOD} is defined as the actual period of the data rate which can have a range as defined in Section 7.1.9.

7.1.11.1 Data Source Jitter

The source of data can have some variation (jitter) in the timing of edges of the data transmitted. The time between any set of data transitions is $N * T_{PERIOD} \pm$ jitter time, where 'N' is the number of bits between the transitions. The data jitter is measured with the same capacitive load used for maximum rise and fall times and is measured at the crossover points of the data lines as shown in Figure 7-17.
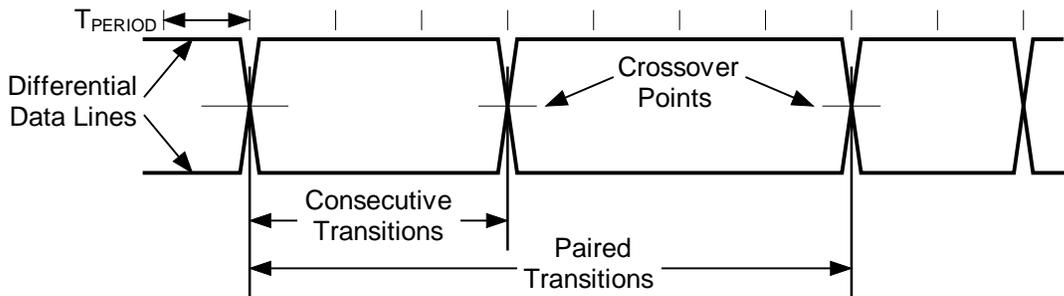

Figure 7-17. Data Jitter

For full speed transmissions, the jitter time for any consecutive differential data transitions must be within ±2.0 ns and within ±1.0 ns for any set of paired differential data transitions. For low speed transmissions, the jitter time for any consecutive differential data transitions must be within ±25 ns and within ±10 ns for any set of paired differential data transitions. These jitter numbers include timing variations due to differential buffer delay and rise/fall time mismatches, internal clock source jitter and to noise and other random effects.

7.1.11.2 EOP Width

The width of the SE0 in the EOP is about $2 * T_{PERIOD}$. The EOP width is measured with the same capacitive load used for maximum rise and fall times and is measured at the same level as the differential signal crossover points of the data lines (see Figure 7-18).
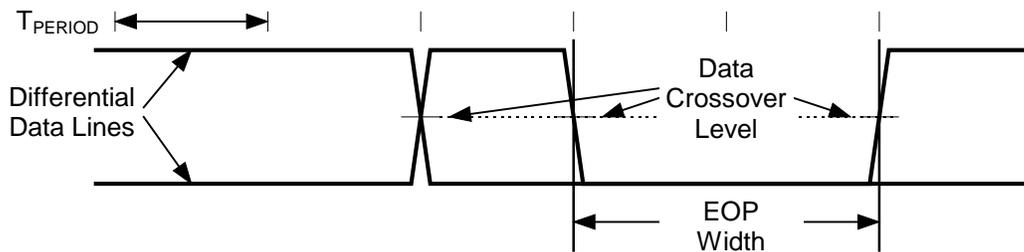

Figure 7-18. EOP Width Timing

For full speed transmissions, the EOP width from the transmitter must be between 160 ns and 175 ns. For low speed transmissions, the transmitter's EOP width must be between 1.25 µs and 1.50 µs. These ranges

include timing variations due to differential buffer delay and rise/fall time mismatches and to noise and other random effects.

The full speed receiver must accept a 82 ns wide SE0 followed by a 'J' transition as a valid EOP. An SE0 narrower than 40 ns or any SE0 not followed by a 'J' transition must be rejected as an EOP. The receiver may reject or accept an EOP between 40 ns and 82 ns as dictated by implementation depending on sampling and synchronization. A low speed receiver must accept a 670 ns wide SE0 followed by a 'J' transition as a valid EOP. An SE0 narrower than 330 ns or an SE0 not followed by a 'J' transition must be rejected as an EOP. An EOP between 330 ns and 670 ns may be rejected or accepted as above. Any SE0 that is 2.5μs or wider is automatically a reset or a disconnect (depending on direction).

7.1.12 Hub Signaling Timings

The propagation of a full speed, differential data signal through a hub is shown in Figure 7-19. The downstream signaling is measured without a cable connected to the port and with a 50 pF capacitive load. The total delay through the cable and hub electronics must be a maximum of 70 ns. If the hub has a USB standard detachable cable, then the delay through hub electronics must be a maximum of 40 ns to allow for a worst case cable delay of 30 ns. The delay through this hub is measured in both upstream and downstream directions as shown in Figure 7-19B, from data line crossover at the input port to data line crossover at the output port.
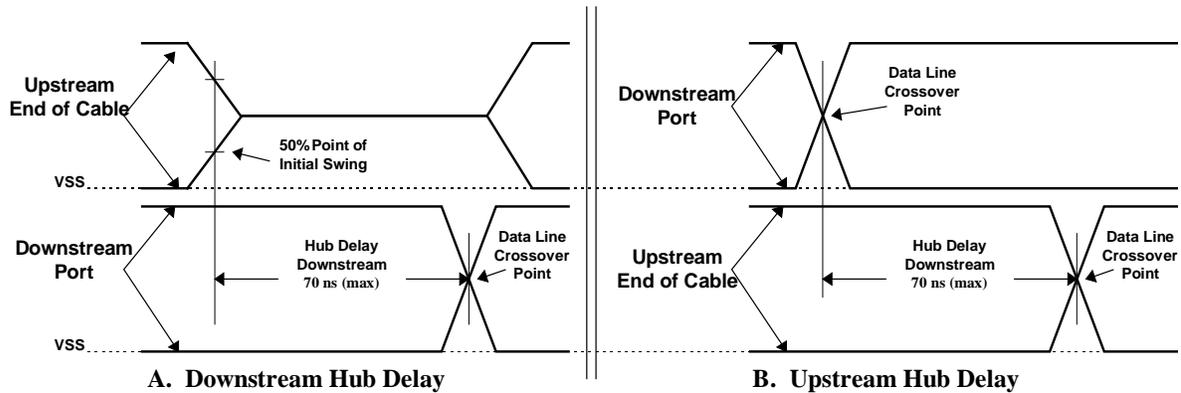

Figure 7-19. Hub Propagation Delay of Full Speed Differential Signals

Low speed propagation delay for differential signals is measured in the same fashion as for full speed signaling. The maximum low speed hub delay is 300 ns. This allows for the slower low speed buffer propagation delay and rise and fall times.

When the hub acts as a repeater, it must reproduce the received signal accurately on its outputs. This means that for differential signals, the propagation delays of a 'J' to 'K' state transition must match closely to the delays of a 'K' to 'J' state transition. The maximum difference allowed between these two delays (as measured in Figure 7-19) for a hub plus cable is ±3.0 ns. Similarly, the difference in delay between any two 'J' to 'K' or 'K' to 'J' transitions through a hub should be less than ±1.0 ns.

An exception to this case is the skew that can be introduced in the SOP idle to 'K' state transition (refer to Section 7.1.4.2). In this case, the delay to the opposite port includes the time to enable the output buffer. However, the delays should be closely matched to the normal hub delay and the maximum additional delay difference over a normal 'J' to 'K' transition is -3.0 ns to +5.0 ns. This limits the maximum distortion of the first bit in the packet. (Note: Because of this distortion of the SOP transition relative to the next 'K' to 'J' state transition, the first sync field bit should not be used to synchronize the receiver to the data stream.)

The EOP has to be propagated through a hub in the same way as the differential signaling. The propagation delay for sensing an SE0 must be no less than the greater of the 'J' to 'K' or 'K' to 'J' differential data delay (to avoid truncating the last data bit in a packet) but not more than 15 ns greater than the larger

differential delay at full speed and 200 ns at low speed (to prevent creating a bit stuff error at the end of the packet). EOP delays are shown in Figure 7-20.

Since the sense levels for the SE0 state are not at the midpoint of the signal swing, the width of the single-ended 0 state will be changed as it passes through each hub. A hub may not change the length of a full speed single-ended 0 state by more than ±15 ns as measured by the difference of the EOP- and EOP+ delays (see Figure 7-20). A single-ended 0 from a low speed device has long rise and fall times and is subject to greater skew, but this conditions exists only on the cable from the low speed device to the port to which it is connected. Thereafter, the signaling uses full speed buffers and their faster rise and fall times. The single-ended 0 from the low speed device cannot be changed by more than ±300 ns as it passes through the hub to which the device is connected. This time allows for some signal conditioning in the low speed port to reduce its sensitivity to noise.
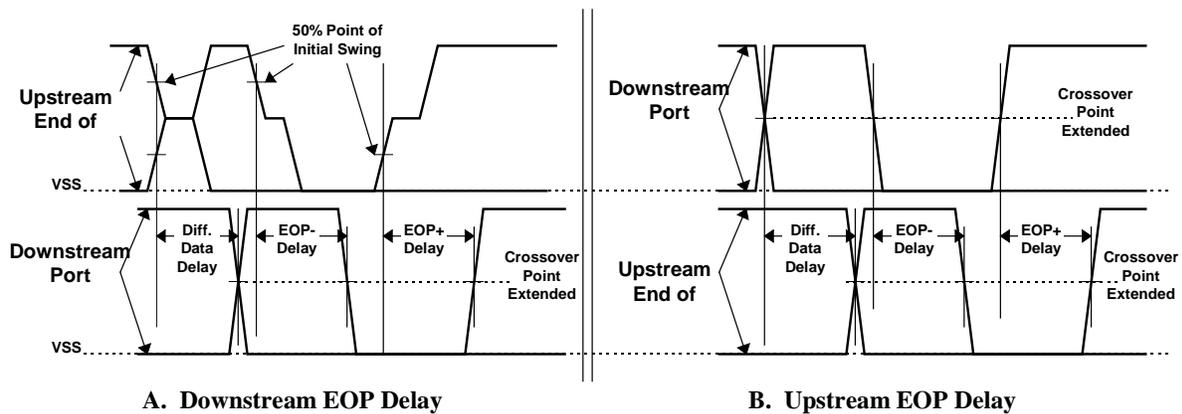

A. Downstream EOP Delay   **B. Upstream EOP Delay**

Figure 7-20. Timing of EOP

7.1.13 Receiver Data Jitter

The data receivers for all types of devices must be able to properly decode the differential data in the presence of jitter. The more of the bit cell that any data edge can occupy and still be decoded, the more reliable the data transfer will be. Data receivers are required to decode differential data transitions that occur in a window plus and minus a nominal quarter bit cell from the nominal (centered) data edge position. (A simple 4X oversampling state machine DPLL can be built that satisfies these requirements.)

Jitter will be caused by the delay mismatches discussed above and by mismatches in the source and destination data rates (frequencies). The receive data jitter budgets for full and low speed are given in Table 7-2 and Table 7-3. These tables give the value and totals for each source of jitter for both consecutive (next) and paired transitions. Note that the jitter component related to the source or destination frequency tolerance has been allocated to the appropriate device (i.e., the source jitter includes bit shifts due to source frequency inaccuracy over the worst case data transition interval). The output driver jitter can be traded off against the device clock accuracy in a particular implementation as long as the jitter specification is met.

The low speed jitter budget table has an additional line in it because the jitter introduced by the hub to which the low speed device is attached is different from all the other devices in the data path. The remaining devices operate with full speed signaling conventions (though at low speed data rate).

Table 7-2. Full Speed Jitter Budget

HUBS   5   F.S. Freq. Tol.   0.0025

MAX BITS/TRANS   7

Jitter Source	Full Speed			
	Next Transition		Paired Transition	
	Each (ns)	Total (ns)	Each (ns)	Total (ns)
Source Driver Jitter	2.0	2.0	1.0	1.0
Source Freq. Tol. - Worst case	0.21/bit	1.5	0.21/bit	3.0
Source Jitter Total		**3.5**		**4.0**
Hub Jitter	3.0	15.0	1.0	5.0
Jitter Spec		**18.5**		**9.0**
Destination Freq. Tol.	0.21/bit	1.5	0.21/bit	3.0
Rcv Jitter Budget		**20.0**		**12.0**

Table 7-3. Low Speed Jitter Budget

HUBS   5   F.S. Freq. Tol.   0.0025

MAX BITS/TRANS   7   L.S. Freq. Tol.   0.015

Jitter Source	Low Speed - Upstream			
	Next Transition		Paired Transition	
	Each (ns)	Total (ns)	Each (ns)	Total (ns)
Function Driver Jitter	25.0	25.0	10.0	10.0
Function Freq. Tol - Worst Case	10.0/bit	70.0	10.0/bit	140.0
Source (Function) Jitter Total		**95.0**		**150.0**
Hub w/ L.S. Device Jitter	45.0	45.0	45.0	45.0
Remaining (F.S.) Hubs' Jitter	3.0	12.0	1.0	4.0
Jitter Spec		**152.0**		**200.0**
Host Freq. Tol.	1.7/bit	12.0	1.7/bit	24.0
Host Rcv Jitter Budget		**164.0**		**225.0**

Jitter Source	Low Speed - Downstream			
	Next Transition		Paired Transition	
	Each (ns)	Total (ns)	Each (ns)	Total (ns)
Host Driver Jitter	2.0	2.0	1.0	1.0
Host Freq. Tol. - Worst Case	1.7/bit	12.0	1.7/bit	24.0
Source (Host) Jitter Total		**14.0**		**25.0**
Hub w/ L.S. Device Jitter	45.0	45.0	15.0	15.0
Remaining (F.S.) Hubs' Jitter	3.0	12.0	1.0	4.0
Jitter Spec		**75.0**		**45.0**
Function Freq. Tol.	10.0/bit	70.0	10.0/bit	140.0
Function Rcv Jitter Budget		**150.0**		**185.0**

Note: This table describes the host transmitting at low speed data rate using full speed signaling to a low speed device through the maximum number of hubs. When the host is directly connected to the low speed device, then it uses low speed data rate and low speed signaling, and the host has to meet the source jitter listed in the "Jitter Spec" line.

7.1.14 Cable Delay

Only one data transition is allowed on a USB cable at a time. A full speed signal edge has to transition, propagate to the far end of the cable, return, and settle within one full speed bit time. Therefore, the maximum allowed cable delay is 30 ns. Independent of cable velocity, the maximum cable length is 5.0 meters for full speed devices and 3.0 meters for low speed devices. The maximum one-way data delay on a cable is measured as shown in Figure 7-21.
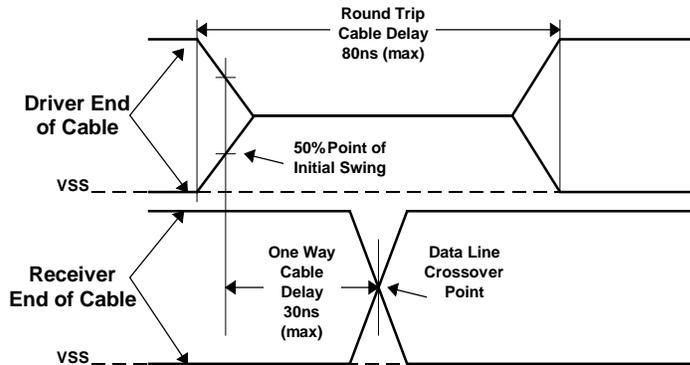
Figure 7-21. Cable Delay

7.1.15 Bus Turnaround Time / Interpacket Delay

A new device may not begin driving the bus until the previous device has completed the EOP sequence and has disabled its drivers. This is assured by not allowing the new device to drive the bus until it has detected that the bus is in the 'J' state after the SE0 in the EOP for at least two bit times. This minimum of two bit times applies to all devices, including back to back host packet transmissions.

If a function is expected to provide a response to a host transmission, the response must be seen on the upstream end of the cable within 7.5 bit times of the bus returning to the 'J' state after the EOP as seen on the upstream end of its cable. The maximum bus turnaround time for a function or hub without an integrated cable is 6.5 bit times. This maximum bus turnaround time prevents a full speed receiving agent from timing out after 16 bit times on a response in a maximum depth topology (refer to Section 7.1.16). However, these timings apply to both full speed and low speed devices.

The maximum delay a host has to respond to a data packet sent by a function (if a handshake is required) is 7.5 bit times, measured at the host's port pins. There is no maximum delay between packets in separate transactions.

7.1.16 Maximum End to End Signal Delay

A device expecting a response to a transmission will invalidate the transaction if it does not see the start of packet (SOP) transition within the time-out period after the end of the transmission (after the SE0 to 'J' state transition in the EOP). This can occur between an IN token and the following data packet or between a data packet and the handshake packet (refer to Chapter 8). The device expecting the response will not time out before 16 bit times and not after 18 bit times measured at the data pins of the device after the end of the EOP. The host will not begin transmission of the token for the next transaction before 18 bit times (measured at its data pins) after it sees the end of a packet with no response.

Figure 7-22 depicts the configuration of six signal hops (cables) that results in worst allowable case signal delay. The maximum propagation delay from the upstream end of a hub's cable to any downstream port connector is 70 ns.
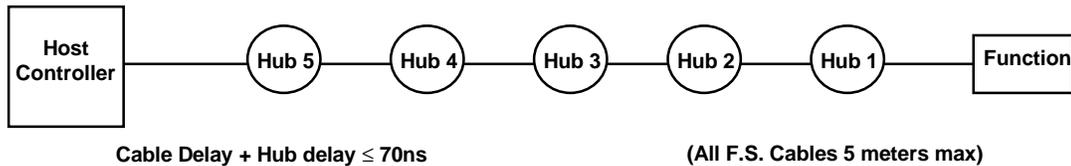

Cable Delay + Hub delay ≤ 70ns   **(All F.S. Cables 5 meters max)**

Figure 7-22. Worst Case End to End Signal Delay Model

7.2 Power Distribution

The power distribution specification for USB is presented in the following paragraphs.

7.2.1 Classes of Devices

The power sourcing and sinking requirements of different device classes can be simplified with the introduction of the concept of a unit load. A unit load is defined to be 100 mA.

USB supports a range of devices as categorized by their power consumption; these include:

- **Bus-powered hubs** - Draws all of the power to any internal functions and downstream ports from the USB connector power pins. May draw up to one load upon power up and a total of five loads, which is split between any embedded functions and external ports. External ports in a bus-powered hub can supply only one load per port regardless of the current drawn on the other ports of that hub.

- **Self-powered hubs** - Power for the internal functions and downstream ports does not come from USB, although the USB interface may draw up to one load from its upstream connection to allow the interface to function when the remainder of the hub is powered down. The hub must supply five unit loads on all of its external downstream ports.

- **Low power, bus-powered functions** - All power to these devices comes from USB connector. They may draw no more than one unit load at any time.

- **High power, bus-powered functions** - All power to these devices comes from USB connector. They must draw no more than one unit load upon power up and may draw up to five unit loads after being configured.

- **Self-powered functions** - May draw up to one load from their upstream connection to allow the interface to function when the remainder of the hub is powered down. All other power comes from an external (to USB) source.

The hub on the host in a desktop computer is a self-powered hub. The same hub in a notebook computer can be defined to be either a self-powered or bus-powered hub.

All devices, whether they are bus-powered or self-powered, can only draw (sink) current from the bus. They must not supply current upstream to a host or hub port. On power up, all devices need to insure that their upstream port is not enabled, so that the device is able to receive the reset signaling, and that the maximum operating current drawn by a device is one unit load. If a device draws power from the bus, its internal supply derived from V_{bus} must be stable within 100 ms of V_{bus} reaching 4.4 V. All devices which are drawing power from the bus must be able enter the suspend state and reduce their current consumption from V_{bus} to less than 500 μA (refer to Section 7.1.4.4 and Section 9.3.5.1).

7.2.1.1 Bus-powered Hubs

The above requirements can be met for bus-powered hubs with a power control circuit as shown in Figure 7-23. Bus-powered hubs often contain at least one embedded function. Power is always available to the hub's controller, which permits host access to power management and other configuration registers during the enumeration process. An embedded function may require that its power be switched, so that upon power-up the entire device (hub and embedded functions) draws no more than one unit load. Power switching on any embedded function may be implemented either by removing its power or by shutting off the clock. Switching on the embedded function is not required if the aggregate power drawn by it and the hub controller is less than one unit load. The total current drawn by an bus-powered device is the sum of the current to the hub controller, any embedded function(s), and the downstream ports.

Figure 7-23 shows the partitioning of power based upon the maximum upstream current of five loads: one unit load for the hub controller and the embedded function, and one load for each of the downstream ports.

The maximum number of downstream ports that can be supported is limited to four. If more ports are required, then the hub will need to be self-powered. If the embedded function(s) and hub controller draw more than one unit load, then the number of ports must be appropriately reduced. Power control to a bus-powered hub may require a regulator. If present, it is always enabled to supply the hub controller. The regulator can also power the embedded functions(s). Inrush current limiting must also be incorporated into the regulator subsystem.
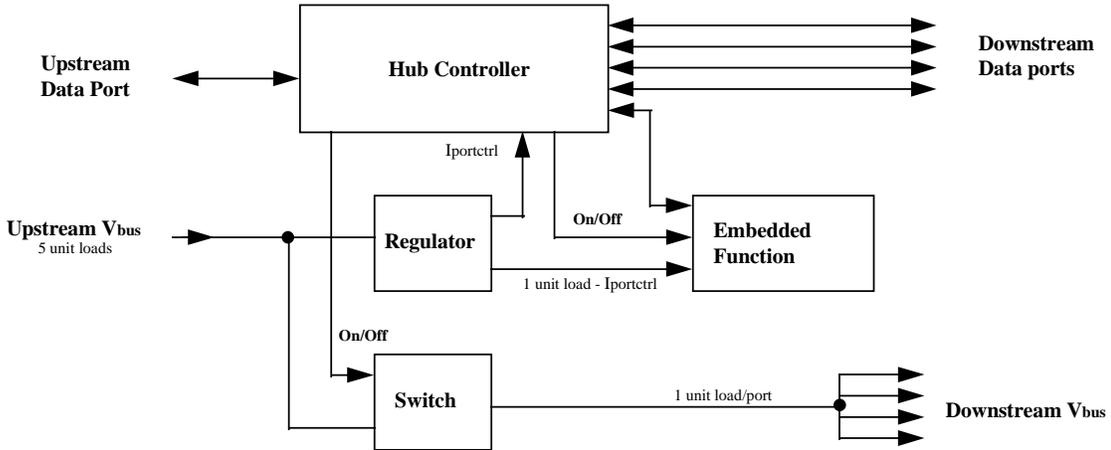

Figure 7-23. Compound Bus-powered Hub

Power to downstream ports must be switched. The hub controller supplies a software controlled on/off signal from the host, which is in the "off" state when the device is powered up or after reset signaling. When switched to the "on" state, the switch implements a soft turn-on function which prevents excessive transient current from being drawn from the upstream port. The voltage drop across the upstream cable, connectors, and switch in an bus-powered hub must not exceed 350 mV at maximum rated current.

7.2.1.2 Self-powered Hubs

Self-powered hubs have a local power supply that furnishes power to any embedded functions and to all downstream ports, as shown in Figure 7-24. Power for the hub controller, however, may be supplied from either the upstream port (a "hybrid" powered hub) or the local power supply. The advantage of supplying the hub controller from the upstream supply is that communication from the host is possible even if the device's power supply remains off. This makes it possible to differentiate between a disconnected and an unpowered device.
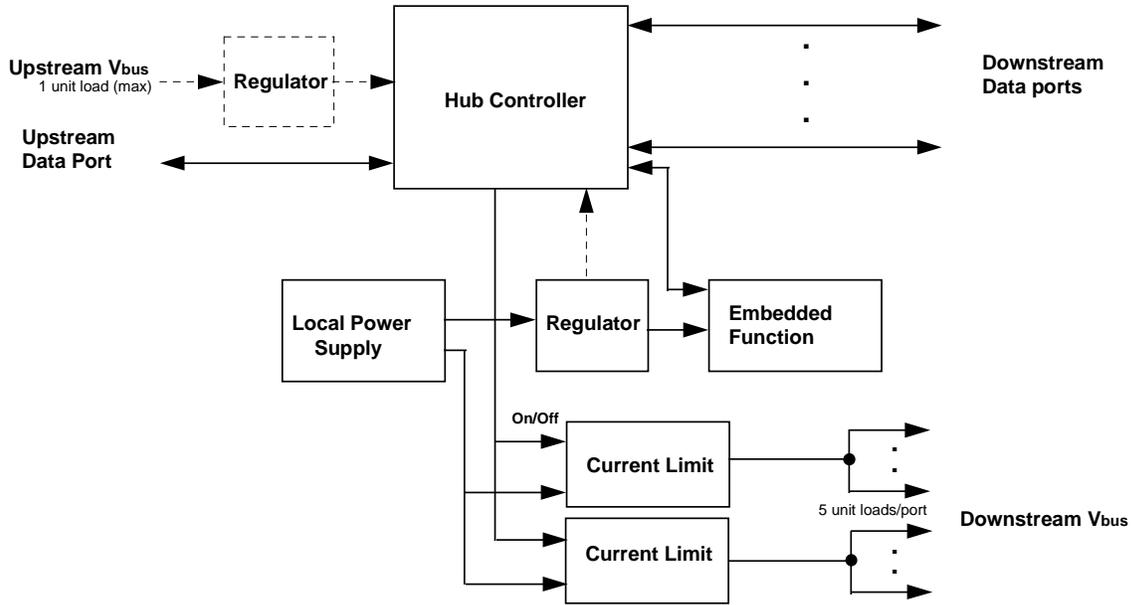
Figure 7-24. Compound Self-Powered Hub

Power is provided to all downstream ports from the local power supply. The number of ports that can be supported is limited only by what the local supply can deliver and by safety concerns. A reasonable maximum is seven ports. Each port must be capable of supplying at least five unit loads. However, no single port can deliver more than 5.0 A in order to meet regulatory safety limits. Current limiting on the downstream ports may need to be partitioned into two or more port subgroups in order to deliver sufficient power to all ports without exceeding the current available through one port. If all seven ports were wired in parallel, the available current at a given port would be $7 * 500$ mA $= 3.5$ A. This is very close to the safety limit. By implementing two current limit circuits, the maximum current that needs to be supplied in operation is reduced to 1.5 A to 2.0 A, which gives a comfortable margin to the safety limit.

7.2.1.2.1 Overcurrent Protection

The host and all self-powered hubs must implement overcurrent protection for safety reasons, and they must have a way to detect the overcurrent condition and report it to the USB software. Should the aggregate current drawn by a group of downstream ports exceed a preset value, the overcurrent protector removes power from all downstream ports and reports the condition through the hub to host controller. The preset value cannot exceed 5.0 A and should be sufficiently above the maximum allowable port current such that power up or dynamic attach transient currents do not trip the overcurrent protector. If an overcurrent condition occurs on any port, subsequent operation of the USB is not guaranteed, and once the condition is removed, it may be necessary to reinitialize the bus as would be done upon power-up. Overcurrent limiting methods can include poly fuses, standard fuses, or some type of solid state switch. The only requirements are that current be limited to five unit loads per port and that the host is notified of an overcurrent condition.

Current limiting should not occur even if illegal topologies are configured, due to the protection afforded by power switching in high power functions and bus-powered hubs. Instead, the overcurrent circuits are used to protect from catastrophic device failures, software errors that turn on devices when the current budget has been exceeded, and user actions such as shorting out the connector pins.

7.2.1.2.2 Power Supply Isolation

Figure 7-24 is based on the assumption that the local power supply shares a common ground with the upstream and downstream ports. Its V_{bus}, however, is isolated from the V_{bus} of the upstream port. There is an additional requirement that the chassis ground (if one exists) of the self-powered hub be DC isolated from the USB signal ground. Chassis ground connects to the ground of a 120 Vac power cable, and there is no guarantee that AC grounds from two different outlets are at the same potential. Failure to observe this precaution could result in large low frequency currents running through USB ground paths.

7.2.1.3 Low-Power, Bus-Powered Functions

A low power function is one that draws less than one unit load from the USB cable when fully operational. The regulator block must both limit inrush current and supply the necessary voltage for the proper signaling levels. Figure 7-25 shows a typical bus-powered low power function, such as a mouse. Low power regulation can be integrated into the function silicon. For higher currents, in the range of 20 mA to 100 mA, an IC linear regulator may be used. Low power functions must be capable of operating with input Vbus voltages as low as 4.40 V measured at the plug end of the cable.
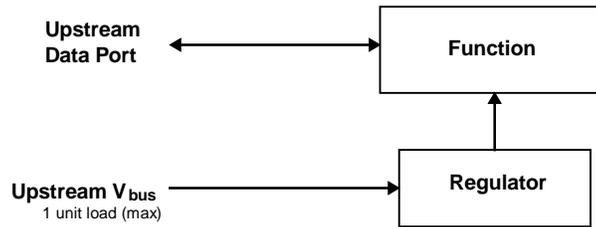
Figure 7-25. Low-Power Function

7.2.1.4 High-Power, Bus-Powered Functions

A function is defined as being high powered if, when fully powered, it draws over one and a maximum of five unit loads from the USB cable. A high-power function requires staged switching of power. It must first come up in a reduced power state of less than one unit load. At bus enumeration time, its total power requirements are obtained and compared against the available power budget. If sufficient power exists in the power budget, the remainder of the function may be powered on. If insufficient power is available, the remainder of the function is not powered and a power limit warning message is sent to the client. A high-power function is shown in Figure 7-26. The function's electronics have been partitioned into two sections; the function controller contains the minimum amount of circuitry necessary to permit enumeration and power budgeting. The remainder of the function resides in the function block. High power functions must be capable of operating in their low power (one unit load) mode with an input voltage as low as 4.40 V, so that it will work even when plugged into an bus-powered hub. They must also be capable of operating at full power (up to five unit loads) with an input Vbus voltage of 4.75 V measured at the upstream plug end of the cable.
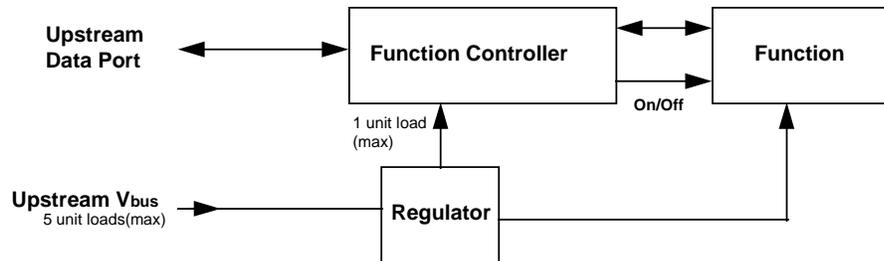
Figure 7-26. High-Power, Bus-Powered Function

7.2.1.5 Self-powered Functions

Figure 7-27 shows a self-powered function. The function controller is powered either from the upstream bus via a low power regulator or from the local power supply. The advantage of the former scheme is that it permits detection and enumeration of a self-powered function whose local power supply is turned off. When the function controller is externally powered, the maximum upstream power that it can draw is one unit load, and the regulator block must implement inrush current limiting. The amount of power that the function block may draw is limited only by the local power supply. Because the local power supply is not required to power any downstream bus ports, it does not need to implement current limiting, soft start, or power switching.

Self-powered functions must adhere to the same ground and V$_{bus}$ isolation rules as self-powered hubs.
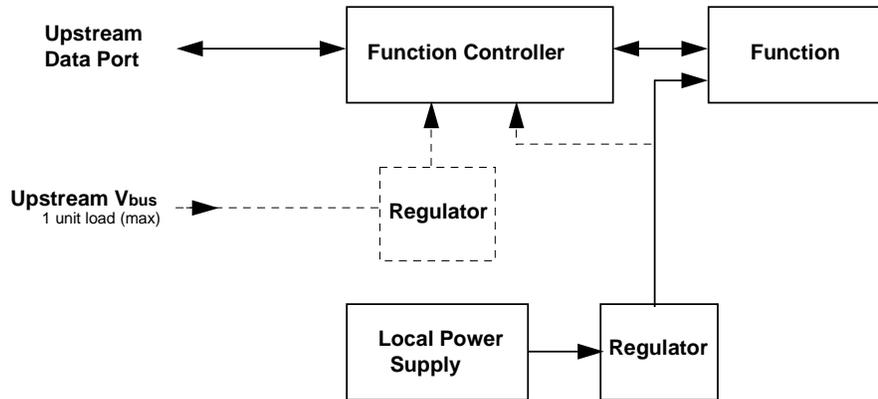

Figure 7-27. Self-powered Function

7.2.2 Voltage Drop Budget

The voltage drop budget is determined from:

- The voltage supplied by host or powered hub ports is 4.75 V to 5.25 V.

- Bus-powered hubs can have a maximum drop of 350 mV from their cable plug where they attach to a source of power to their output port connectors where they supply a source of power.

- All hubs and functions must be able to provide configuration information with as little as 4.40 V at the connector end of their upstream cables. Only low power functions need to be able to be fully operational with this minimum voltage.

- Functions drawing more than one unit load must operate with a 4.75 V minimum input voltage at the connector end of their upstream cables.

Figure 7-28 shows the minimum allowable voltages in a worst case topology consisting of an bus-powered hub driving an bus-powered function.
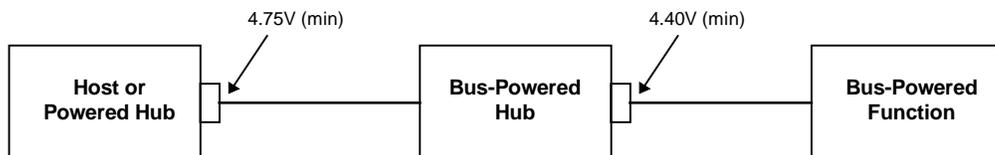

Figure 7-28. Worst Case Voltage Drop Topology

These requirements place stringent restrictions on cable and connector IR drops (refer to Section 6.4) and port switch drops. However, they should be achievable with existing technologies at a reasonable cost.

7.2.3 Dynamic Attach and Detach

The act of plugging or unplugging a hub or function does not affect the functionality of another device on other segments of the network. Unplugging a function will stop the transaction between that function and the host. However, the hub to which this function was attached will recover from this condition and will alert the host that the port has been disconnected.

7.2.3.1 Inrush Current Limiting

When a function or hub is plugged into the network, it has a certain amount of on-board capacitance between Vbus and ground. Also, the regulator will supply current to its output bypass capacitance and to the function as soon as power is applied. As a result, if no measures are taken to prevent it, there can be a surge of current into the device sufficient to pull the Vbus on the hub below its minimum operating level. Inrush currents can also occur when a high power function is switched into its high power mode. This problem must be solved by limiting the inrush current and by providing sufficient capacitance in each hub to prevent the power supplied to the other ports from going out of tolerance. An additional motivation for limiting inrush current is to minimize contact arcing, thereby prolonging connector contact life.

The target maximum droop in the hub Vbus is 330 mV or about 10% of the nominal signal swing from the function. In order to meet this target, the following conditions must be met:

- The maximum load that can be placed at the downstream end of a cable is 10 µF in parallel with 44 Ω. The 10 µF capacitance represents any bypass capacitor directly connected across the Vbus lines in the function plus any capacitive effects visible through the regulator in the device. The 44 Ω resistor represents one unit current load generated by the device during connect.

- If more bypass capacitance is required in the device due to large swings in the load current, then the device must incorporate some form of surge current limiting for current in the cable such that it matches the characteristics of the above load.

- The hub port Vbus power lines must be bypassed with no less than a 120 µF tantalum capacitor (equivalent aluminum capacitor values are under test) . Good standard bypass methods should be used to minimize inductances between the bypass capacitors and the connectors. The bypass capacitors themselves should have a low dissipation factor to allow decoupling at higher frequencies.

The upstream port of a hub is also required to meet the above requirements. Furthermore, a bus-powered hub must provide additional surge limiting in the form of a soft start circuit when it enables power to its downstream ports.

Signal pins are protected from excessive currents during dynamic attach by being recessed in the connector such that the power pins make contact first. This guarantees that the power rails to the downstream device are referenced before the signal pins make contact. Also, the hub port signal lines are disabled and in a high impedance state during connect, allowing no current to flow for standard signal levels.

7.2.3.2 Dynamic Detach

When a device is detached from the network with power flowing in the cable, the inductance of the cable will cause a large flyback voltage to occur on the open end of the device cable. This flyback voltage is not destructive. Proper bypass measures on the hub ports will suppress any coupled noise. The frequency range of this noise is inversely dependent on the length of the cable to a maximum of 60 MHz for a one meter cable. This will require some low capacitance, very low inductance bypass capacitors on each hub port connector. The flyback voltage and the noise it creates is also moderated by the bypass capacitance on the device end of the cable. Also, there must be some minimum capacitance on the device end of the cable to insure that the inductive flyback on the open end of the cable does not cause the voltage on the device end to reverse polarity. A minimum of 1.0 µF is recommended for bypass across Vbus.

Again, signal pins are protected from excessive voltages during dynamic detach by being recessed in the connector such that they break contact before the power pins.

7.3 Physical Layer

The physical layer specifications are described in the following subsections.

7.3.1 Environmental

The operating environment for USB is 0 °C to 70 °C ambient.

USB must meet the following regulatory requirements;

EMI:

FCC part 15 class B

EN55022:1994 (Based on CISPR-22:1993)

EN5082-1:1992 (Generic Immunity standard)

VCCI (Japan version of CISPR-22)

Safety:

UL, CSA

7.3.2 Bus Timing/Electrical Characteristics

Table 7-4. DC Electrical Characteristics

Parameter	Symbol	Conditions (Notes 1,2)	Min.	Max.	Unit
Supply Voltage:					
Powered (Host or Hub) Port	VBUS		4.75	5.25	V
Bus-powered Hub Port	VBUS		4.40	5.25	V
Supply Current:					
Powered Host/Hub Port (out)	ICCPRT		500		mA
Bus-powered Hub Port (out)	ICCUPT		100		mA
High Power Function (in)	ICCHPF			500	mA
Low Power Function (in)	ICCLPF			100	mA
Unconfig. Function / Hub (in)	ICCINIT			100	mA
Suspended Device	ICCS			500	µA
Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V< V_{IN}<3.3 V	-10	+10	µA
Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|, and Figure 7-4	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Ended Receiver Threshold	VSE		0.8	2.0	V
Output Levels:					
Static Output Low	VOL	RL of 1.5 kΩ to 3.6 V		0.3	V
Static Output High	VOH	RL of 15 kΩ to GND	2.8	3.6	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Downstream Hub Port Bypass Capacitance	CHPB	Vbus to GND (Tantalum)	120		µF
Root Port Bypass Capacitance	CRPB	Vbus to GND Note 9	1.0	10.0	µF
Terminations:					
Bus Pull-up Resistor on Root Port	RPU	(1.5 kΩ ± 5%)	1.425	1.575	kΩ
Bus Pull-down Resistor on Downstream Port	RPD	(15 kΩ ± 5%)	14.25	15.75	kΩ
Cable Impedance and Timing:					
Cable Impedance (Full Speed)	ZO	(45 Ω ±15%)	38.75	51.75	Ω
Cable Delay (one way)	TCBL	Figure 7-21		30	ns

Table 7-5. Full Speed Source Electrical Characteristics

Parameter	Symbol	Conditions (Notes 1,2,3)	Min.	Max.	Unit
Driver Characteristics:					
Transition Time:		Note 5, 6 and Figure 7-16			
Rise Time	TR	CL = 50 pF	4	20	ns
Fall Time	TF	CL = 50 pF	4	20	ns
Rise / Fall Time Matching	TRFM	(TR/TF)	90	110	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Driver Output Resistance	ZDRV	Steady State Drive	28	43	Ω
Data Source Timings:					
Full Speed Data Rate	TDRATE	Ave. Bit Rate (12Mb/s ± 0.25%)	11.97	12.03	Mbs
Frame Interval	TFRAME	1.0 ms ± 0.05%	0.9995	1.0005	ms
Source Differential Driver Jitter		Note 7, 8			
To Next Transition	TDJ1	and Figure 7-29	-3.5	3.5	ns
For Paired Transitions	TDJ2		-4.0	4.0	ns
Source EOP Width	TEOPT	Note 8 and Figure 7-30	160	175	ns
Differential to EOP transition Skew	TDEOP	Note 8 and Figure 7-30	-2	5	ns
Receiver Data Jitter Tolerance		Note 8 and Figure 7-31			
To Next Transition	TJR1		-18.5	18.5	ns
For Paired Transitions	TJR2		-9	9	ns
EOP Width at receiver		Note 8 and Figure 7-30			
Must reject as EOP	TEOPR1		40		ns
Must accept as EOP	TEOPR2		82		ns

Table 7-6. Low Speed Source Electrical Characteristics

Parameter	Symbol	Conditions (Notes 1,2,4)	Min.	Max.	Unit
Driver Characteristics:					
Transition Time:		Note 5, 6 and Figure 7-16			
Rise Time	TR	CL = 50 pF	75		ns
		CL = 350 pF		300	ns
Fall Time	TF	CL = 50 pF	75		ns
		CL = 350 pF		300	ns
Rise / Fall Time Matching	TRFM	(TR/TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave. Bit Rate (1.5Mb/s ± 1.5%)	1.4775	1.5225	Mbs
Source Differential Driver Jitter		Note 7, 8			
Host (Downstream):		and Figure 7-29			
To Next Transition	TDDJ1		-75	75	ns
For Paired Transitions	TDDJ2		-45	45	ns
Function (Upstream):					
To Next Transition	TUDJ1		-95	95	ns
For Paired Transitions	TUDJ2		-150	150	ns
Source EOP Width	TEOPT	Note 8 and Figure 7-30	1.25	1.50	µs
Differential to EOP transition Skew	TDEOP	Note 8 and Figure 7-30	-40	100	ns
Receiver Data Jitter Tolerance		Note 8 and Figure 7-31			
At Host (Upstream):					
To Next Transition	TUJR1		-152	152	ns
For Paired Transitions	TUJR2		-200	200	ns
At Function (Downstream):					
To Next Transition	TDJR1		-75	75	ns
For Paired Transitions	TDJR2		-45	45	ns
EOP Width at receiver		Note 8 and Figure 7-30			
Must reject as EOP	TEOPR1		330		ns
Must accept	TEOPR2		675		ns

Table 7-7. Hub / Repeater Electrical Characteristics

Parameter	Symbol	Conditions (Note 2)	Min.	Max.	Unit
Hub Characteristics (Full Speed):					
Driver Characteristics (Refer to Table 7-5)		Root port and Downstream ports configured as Full Speed			
Hub Differential Data Delay (with cable) (without cable)	THDD1 THDD2	Note 3, 7, 8 and Figure 7-32		70 40	ns ns
Hub Differential Driver Jitter (including cable) To Next Transition For Paired Transitions	THDJ1 THDJ2	Note 3, 7, 8 and Figure 7-32	-3 -1	3 1	ns ns
Data bit width distortion after SOP	TSOP	Note 3, 8 and Figure 7-32	-5	3	
Hub EOP Delay Relative to t_{HDD}	TEOPD	Note 3, 8 and Figure 7-33	0	15	ns
Hub EOP Output Width Skew	THESK	Note 3, 8 and Figure 7-33	-15	15	ns
Hub Timings (Low Speed):					
Driver Characteristics (Refer to Table 7-6)		Downstream ports configured as Low Speed			
Hub Differential Data Delay	TLHDD	Note 4, 7, 8 and Figure 7-32		300	ns
Hub Differential Driver Jitter (including cable) Downstream: To Next Transition For Paired Transitions	TLDHJ1 TLDHJ2	Note 4, 7, 8 and Figure 7-32	-45 -15	45 15	ns ns
Upstream: To Next Transition For Paired Transitions	TLUHJ1 TLUHJ2		-45 -45	45 45	ns ns
Data bit width distortion after SOP	TSOP	Note 4, 8 and Figure 7-32	-60	45	
Hub EOP Delay Relative to t_{HDD}	TLEOPD	Note 4, 8 and Figure 7-33	0	200	ns
Hub EOP Output Width Skew	TLHESK	Note 4, 8 and Figure 7-33	-300	+300	ns

Note 1: All voltages measured from the local ground potential, unless otherwise specified.

Note 2: All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.

Note 3: Full Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D+ data line.

Note 4: Low Speed timings have a 1.5 kΩ pull-up to 2.8 V on the D- data line.

Note 5: Measured from 10% to 90% of the data signal.

Note 6: The rising and falling edges should be smoothly transitioning (monotonic).

Note 7: Timing difference between the differential data signals.

Note 8: Measured at crossover point of differential data signals.

Note 9: The maximum load specification is the maximum effective capacitive load allowed that meets the target
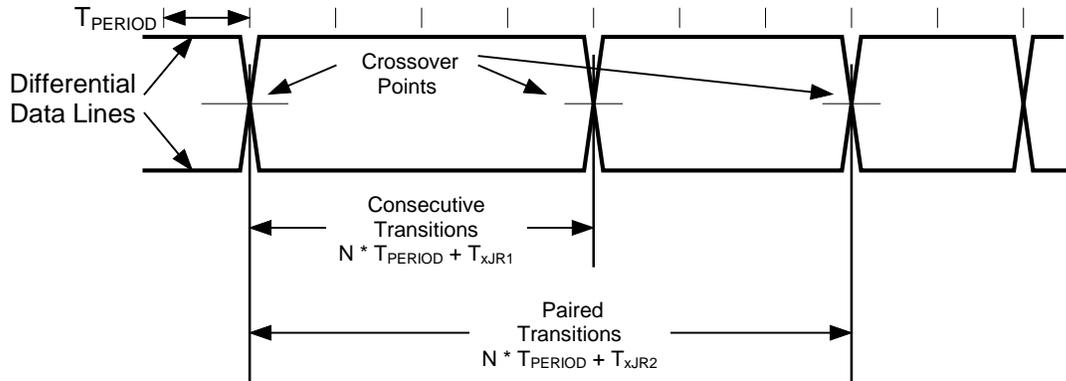hub V_{BUS} droop of 330 mV.

7.3.3 Timing Waveforms
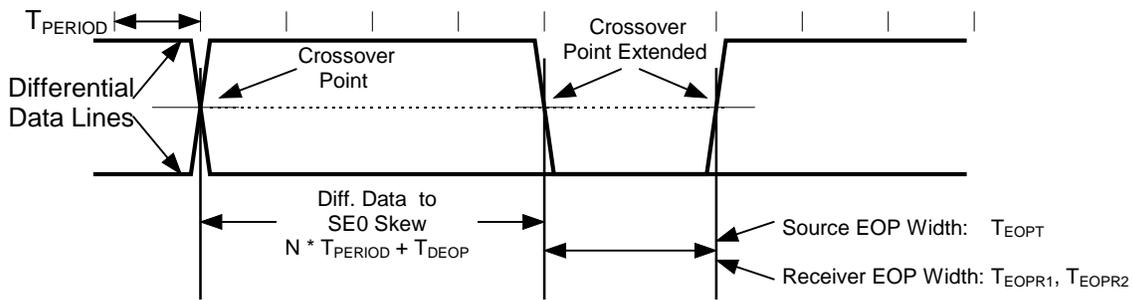

Figure 7-29. Differential Data Jitter

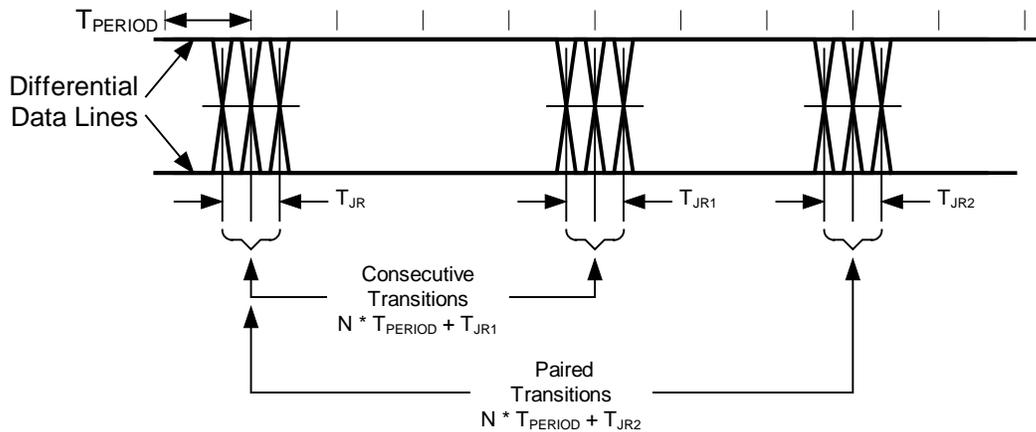**Figure 7-30. Differential to EOP Transition Skew and EOP Width**

Figure 7-31. Receiver Jitter Tolerance.

Refer to Section 7.1.11 for the definition of T_{PERIOD}

**A. Downstream Hub Delay**   **B. Upstream Hub Delay**
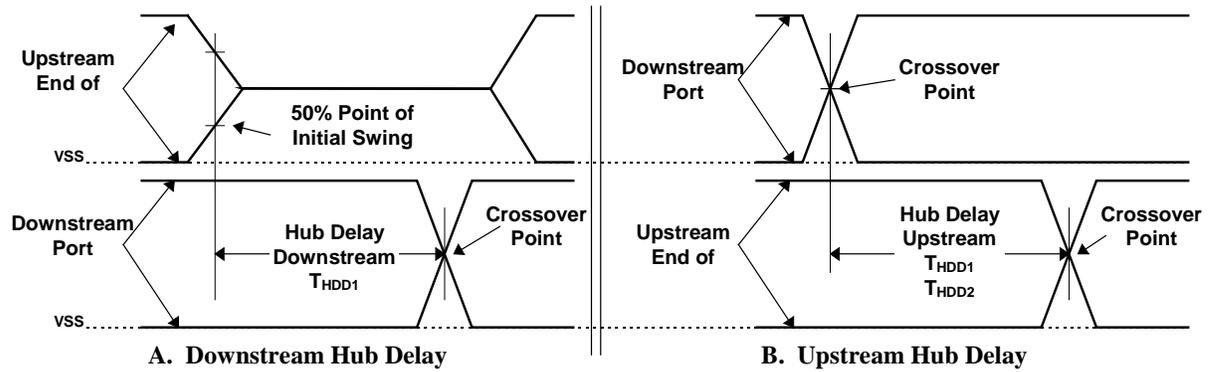
Hub Differential Jitter:

$T_{HDJ1} = T_{HDDx}(J) - T_{HDDx}(K)$ or $T_{HDDx}(K) - T_{HDDx}(J)$ **Consecutive Transitions**

$T_{HDJ2} = T_{HDDx}(J) - T_{HDDx}(J)$ or $T_{HDDx}(K) - T_{HDDx}(K)$ **Paired Transitions**

Bit after SOP Width Distortion: (Same as data jitter for SOP and next J transition.)

$T_{HDJ1} = T_{HDDx}(SOP) - T_{HDDx}(next\ J)$

Low Speed timings are determined in the same way for:

T_{LHDD}, T_{LDHJ1}, T_{LDJH2}, T_{LUHJ1}, T_{LUJH2}, and T_{LSOP} .

Figure 7-32. Hub Differential Delay, Differential Jitter, and SOP Distortion

A. Downstream EOP Delay   **B. Upstream EOP Delay**
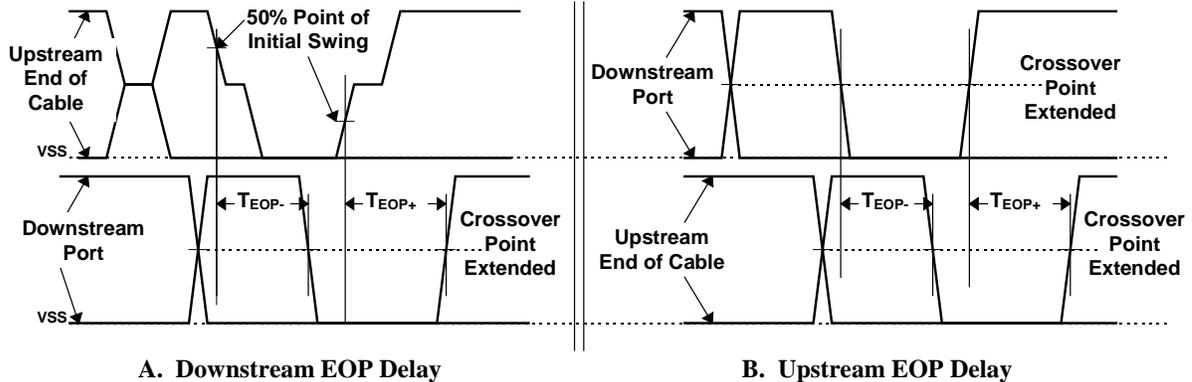
EOP Delay

$T_{EOPD} = T_{EOP-}$

EOP Skew

$T_{HESK} = T_{EOP+} - T_{EOP-}$

Low Speed timings are determined in the same way for:

T_{LEOPD} and T_{LHESK}

Figure 7-33. Hub EOP Delay and EOP Skew