TRF2020

QUESTION: How much current does the TRF2020 draw when operated at 3.0 V?
ANSWER: It draws 10.0 mA at 3.0V versus 11 mA when biased at 4.5V.

QUESTION: Are any of the loop bandwidths effected by operating at 3.0V?
ANSWER: The tuning voltage available to the VCO will be limited by this VDDA setting. However, the VCO must require a tuning voltage to match the available tuning range. The loop filter design should also take into account the available tuning range.

QUESTION: What phase detector comparison frequency is employed for Figure 19 on page 17 of the datasheet?
ANSWER: The phase detector comparison frequency used for the plot shown in Figure 19 of the TRF2020 datasheet is 200 kHz. The loop filter on the TRF2020 EVM was optimized for the 200 kHz comparison frequency. With the 200 kHz comparison frequency, the channel switching time between 1074 MHz and 1109 MHz is approximately 0.8 mS. The TRF2020 was developed for GSM applications which require a 200 kHz channel spacing. The phase detector comparison frequency must thus be set at a multiple of 200 kHz. Ideally, the phase comparison frequency should be set at 200 kHz (1x multiple). The TRF2020 application board has been verified at comparison frequencies of 400 kHz and 800 kHz with the same loop filter which was optimized for the 200 kHz comparison frequency. Results show similar switching-time performance when compared to the 200 kHz case, except that the VCO exhibits an increase in phase noise. This increase in phase noise is due solely to the higher comparison frequency and the non-optimized loop filter.

QUESTION: If a 30 kHz phase detector comparison frequency is employed, what would be the switching speed for frequency shift from 1074 MHz to 1109 MHz? One realizes that this is governed in part by the loop filter but would like an answer in context of current filter as well as discussion of impact of changes to loop filter.
ANSWER: If you do not make any changes to the loop filter and set the phase detector frequency to 30 kHz, the time required to lock (within +/- 1 kHz) when switching from 1074 MHz to 1108.98 MHz is very close to 6 ms (+/- 0.3 ms)
You should redesign the loop filter for the following two reasons:
1) Due the wide (7-8 kHz) bandwidth of the loop filter, the 30 kHz frequency spurs are not attenuated more than ~55 dBc (which in most communication systems would not be adequate.)
2) The switching time is much longer than it needs to be. With the loop filter designed for a 2 kHz bandwidth (to attenuate the 30 kHz spurs) and 30 kHz phase detector frequency, the following component values were arrived at by the author:
C18 = 1000 pF, R22 = 33 kΩ, C6 = 0.01μF, R19 = 150 kΩ, C16 = 100 pF
This design resulted in >66 dBc rejection of the 30 kHz spur and demonstrated a lock time of 3 ms when switching from 1074 MHz to 1108.98 MHz.